The Continuing Dangers of Tin Whiskers and Attempts to Control Them with Conformal Coating

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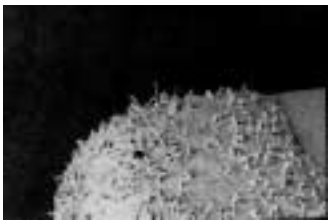
Figure 1. SEM photo of a tin whisker breaking out from beneath conformal coating (x625)

Abstract:
A 1998 commercial satellite failure caused by tin whisker induced shorts prompted NASA Goddard Space Flight Center (GSFC) to issue a NASA Advisory (NA-044 and NA-044A) [(1,2)] to remind the NASA community of the tin whisker phenomenon and the inherent risks associated with the use of pure tin plated components. Indeed the NASA Advisory served as a "reminder" since the spontaneous growth of tin whiskers from some tin plated surfaces has been known and studied for over 50 years with dozens of technical publications and several GIDEP Alerts produced during that time. During the 1990s the US Military modified most (but not all) of their electronic component specifications to prohibit the use of pure tin finishes in order to minimize the risks of whiskering. However, as regulations and a world economy push today's electronics industry to use environmentally friendly (Pb-free) alternatives, the prevalence of pure tin plated components is bound to increase potentially increasing NASA's risk of exposure to risks associated with tin whiskers significantly.

In an effort to evaluate risk mitigation techniques, NASA GSFC initiated experiments to study the effects of Uralane 5750 (a commonly used conformal coat) on tin whisker growth. After more than two years of experimentation, we have found that conformal coat does not prevent tin whisker formation although it does appear to substantially reduce the rate of growth. We have observed that a tin whisker has grown through an area of conformal coat that is approximately 1/4 mil thick (see figure 1). Numerous tin nodules growing beneath a nominal 2 mil thick coating are also being monitored to determine if and when they will be able to penetrate this barrier. We have also observed that tin whiskers can bend in response to forces of electrostatic attraction; thus increasing the probability of tin whisker shorts either from two whiskers colliding or from one whisker bending to contact another conductor. Especially for long duration missions, use of conformal coat as a sole means of risk mitigation may not be completely effective. Research is ongoing.

BACKGROUND:
The growth of tin whiskers on pure tin plated electronic components and associated hardware has been documented for decades. Notable examples of pure tin plated components that have exhibited tin whisker formations include electromagnetic relays, transistors, hybrid microcircuit packages, terminal lugs and very recently ceramic chip capacitors. A few such examples are shown below in figure 2:



Electromagnetic relay terminals	Ceramic chip capacitor termination	Hybrid microcircuit lid
Photo courtesy of NASA GSFC	*Photo courtesy of Ericsson*	*Photo courtesy of JPL*

Figure 2. Examples of Tin Whiskers Growing on Pure Tin Plated Electronic Components

An article was published in the December 1998 edition of the EEE Links Newsletter that provides a basic overview of the tin whisker phenomenon and some of the inherent risks.[3] Included in that article are explanations of the possible effects of tin whiskers in more conventional earth-based environments. Also, interim results and a detailed explanation of GSFC experiments were reported in a September 2000 paper entitled “Effect of Conformal Coat on Tin Whisker Growth”.[4] The authors of this current article guide interested readers to these two publications for a simple primer on tin whiskers and details of the GSFC experimental process as those details will not be repeated here. In addition, the NASA Goddard Tin Whisker Homepage provides an extensive list of reference materials on the topic as well as access to our published paper:

http://nepp.nasa.gov/whisker

A 1998 on-orbit commercial satellite failure was reportedly caused by tin whiskers emanating from the surface of a pure tin plated relay.[5] Over time the whiskers grew to such a length that they were capable of short circuiting the spacecraft bus. Laboratory tests dating back to the early 1990s demonstrated the potential for a tin whisker short to form a plasma in reduced barometric pressure environments (vacuum).[6,7] If sufficient energy and a low impedance path are available from the power source, this plasma can sustain an arc that is capable of carrying HUNDREDS of AMPERES! Such a short circuit is reported to have occurred on the commercial satellite opening protective fuse elements thus rendering the spacecraft non-operational. Since 1998 it has been reported that two additional commercial satellites employing a similar bus design have failed from this same mechanism.[8]

Despite the extensive research performed to date by industry and academia, an accepted comprehensive description of the growth mechanism(s), effective risk mitigation practices and industry accepted tin whisker test methods still elude researchers. It is however, commonly believed that the whiskers form in order to relieve residual stresses in the plating that result from internal and/or external stresses. As such, "bright" tin finishes which have a high residual stress after plating are more prone to whiskering. Numerous other factors also affect whiskering propensity such as substrate material, plating chemistry and process, plating thickness and grain size. The studies to date have not conclusively demonstrated the relative importance of these factors nor combinations of these factors and as such a "proven" whisker-free pure tin plating process that is adaptable to all types of components is not yet available.

Some studies suggest that alloying as little as 0.9% lead (Pb) with the tin dramatically reduces the size and growth rate of whiskers to a low enough level that is safe for current microelectronic geometries. As such, NASA Advisory NA-044 reports that the most effective risk mitigation technique against tin whisker induced short circuits is to prohibit the use of electronic components and associated hardware that employ pure tin plating as a final surface finish (common practice is to require a minimum of 3% Pb). The current worldwide initiative to reduce the use of potentially hazardous materials such as Pb is driving the electronics industry to consider pure tin plating as an alternative to tin-lead plating. With respect to factors such as solderability, ease of manufacture and compatibility with existing assembly methods pure tin plating is a viable alternative. However, the current lack of an industry accepted understanding of tin whisker growth factors and/or test methods to identify whisker-prone products makes a blanket acceptance of pure tin plating a risky proposition for high reliability systems.

Knowing that simple prohibition of pure tin plating will become more and more difficult, NASA GSFC decided to conduct experiments to study the effectiveness of other tin whisker risk mitigation techniques. Several mitigation approaches have been suggested in the past including annealing or reflowing the plated surface with high temperature to relax internal stresses, covering solderable surfaces with a Pb-containing solder or coating the surface with a protective barrier of conformal coat. All of these practices have benefits and limitations. The conformal coat approach seemed to be the most practical and least invasive technique for high reliability systems. GSFC review of the available literature found limited information related to the benefits of conformal coating as a risk mitigation technique. Therefore, in December 1998 NASA GSFC began experiments to evaluate the effectiveness of using conformal coat to mitigate the risk of tin whisker growth.

Experimental Approach:

The objective of the GSFC experiments was to determine if conformal coat could be used as an effective risk mitigator, when whisker-prone (or unknown whisker propensity) components are used in electronic systems.

Uralane 5750 was selected as the conformal coat material for these experiments because of its common use in NASA flight hardware. Experiments were devised to evaluate the effectiveness of Uralane 5750 at:

- **Delaying the onset** of tin whisker formation (incubation period)
- **Affecting the growth rate** of tin whiskers
- **Affecting the growth density** of tin whiskers
- **Preventing tin whiskers from growing through the coating**

As such, for the purpose of these experiments, test specimens with extremely high propensity to form tin whiskers were intentionally produced, so that the effects of the coating on whiskering could be observed and documented. A literature search found that brass substrates with "bright" tin electroplate of approximately 200 microinches were highly prone to whisker formation. The specimens for our experiments were procured from a commercial plating shop.

- Substrate Material: Brass Type 260 (test coupons were 4" x 1" x 0.032")
- Underplate: 50% of samples have a copper strike and copper plate to 0.0001" min
  50% of samples have NO underplate (i.e., tin plate direct on brass)
- Plating Process: "Bright" tin bath
- Tin Plate Thickness: 200 ± 50 microinches

To further promote whisker formation, portions of the test specimens were intentionally scratched using a knife blade. Such surface defects are reported to create localized stresses in the plating that may promote whisker formation. Samples were then coated over half their surface using Uralane 5750 to a nominal thickness of 2 mils; the other half was left uncoated as a control. Seven (7) samples were stored under ambient laboratory conditions (approximately 22°C and 30% to 70% relative humidity) while eight (8) samples were stored at 50°C which our literature review found to be commonly reported as the optimal temperature for whisker formation.

Experimental Results/Observations After 2 ½ Years:

For the last 2 ½ years the test specimens have been examined periodically, using both optical techniques and scanning electron microscopy (SEM).

Incubation Period and Whisker Density:
Our experiments to date have shown that Uralane 5750 conformal coat applied over top of whisker-prone test specimens does NOT PREVENT the formation of tin whiskers. Tin nodules initiated within one month of plating on both the conformal coated and non-coated specimens. Interestingly, after 4 months, the density of the nodules was 4 to 5 times higher on the coated side compared to the non-coated side. However, one year after the initiation of the experiment the density of whisker formations was found to be approximately equal on both coated and non-coated specimens. It was hypothesized that the rapid formation of tin oxide on the non-coated side increases the incubation period for whisker formation. This hypothesis has not been tested.

Figure 3 shows the formation of tin nodules beneath the conformal coat on several specimens. Such growths under the conformal coating are common on all of the specimens regardless of storage conditions (room temperature vs. 50°C). In these SEM images the tin whiskers resemble a spike being pushed into a rubber membrane, deforming the surface into a sharp-tipped cone. It is interesting to observe that many of the whiskers in Figure 3 formed along a surface scratch or defect in the substrate that was NOT intentionally introduced. These minor defects were most likely present on the substrate prior to plating or were introduced through the handling of the specimens just prior to initiation of the experiments. This observation raises the concern that basic handling during manufacturing or user assembly may impart stresses to the plating surface which become nucleation sites for whisker growths.



10X magnification *43X magnification* *670X magnification*

Figure 3. SEM photos of tin domes forming beneath conformal coating

Whisker Growth Rate:

The application of conformal coat appears to retard the rate of whisker growth compared to an uncoated surface. The longest whisker observed on these specimens on the non-coated side is on the order of 2 mm, whereas those whiskers growing beneath the conformal coat are on the order of 0.05 mm (at present). Still unknown is whether the rate of growth will increase once the whisker has broken through the coating material. The average growth rate of the needle-like whiskers on the non-conformally coated areas is about 0.13 mm/year. The fastest growth rate from these specimens is approximately 0.80 mm/year.

Whisker Penetration of Conformal Coating:

Figure 1 shows the most extreme observation we have recorded to date where a tin whisker has actually grown through the conformal coating approximately 2 years after application of the conformal coat. Attempts to measure the actual thickness of the coating at this location have been difficult because this area of the test specimen has a relatively thin layer of conformal coat. Estimates of the coating thickness in this location are on the order of 1/4 mil. After emerging from the coating, the tin whisker can become a risk for inducing short circuits. As noted previously, there are numerous other whisker growths beneath the thicker areas of conformal coating (~ 2 mil thick) that we anticipate will eventually penetrate the conformal coating. With some NASA missions extending over 10 years, and a few to 20 years, it is possible (but not confirmed experimentally) that coatings even as thick as 10 mils may not prevent whiskers from protruding.

Future inspections will continue to look for more whiskers penetrating the coating and if possible, experiments may be conducted to examine the effect of the conformal coating at quenching an arc formed by a whisker induced short circuit under reduced barometric pressure conditions (vacuum).

Demonstration of Whisker Deflection due to Electrostatic Attraction:

Theoretical calculations predict that a whisker that emerges from a coated surface and then comes in contact with a 2nd coated surface will buckle before being able to penetrate that surface.(1) However, short circuits caused by tin whiskers growing outward through a conformal coating are **still a real risk**. Suppose two whiskers emerge from beneath separate conformally coated surfaces at different electrical potentials. **The electrostatic force generated by the potential difference between the whiskers will attract them towards each other thus significantly increasing the likelihood of the whiskers shorting together.** Figure 4 shows tin whisker growing from a mounting tab of a pure tin plated relay. In this GSFC experiment, the mounting tab (and thus the tin whisker) was electrically grounded. A test probe (used to simulate a 2nd whisker) was brought into close proximity (~ 1 mm) of the whisker, but situated such that physical shorting was not possible. The test probe was then placed at 50 V relative to the whisker. As can be seen from this enhanced photo, the tin whisker bends as a result of electrostatic force generated by the potential difference between the whisker and the test probe. After removal of the test potential, the whisker bends back to its original position. This experiment was repeated hundreds of times without causing the whisker to break. Further experiments to study this behavior are planned.

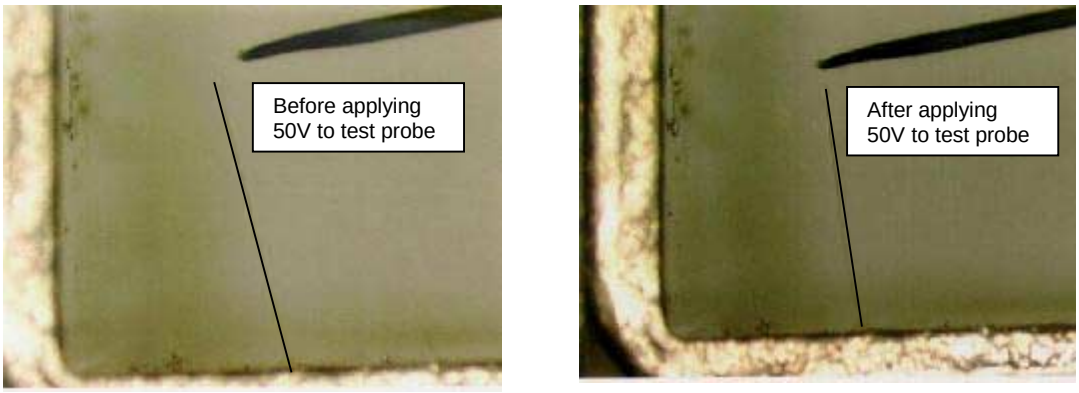


Figure 4. Optical photo of tin whisker movement due to electrostatic attraction
(Note: Photo has been graphically enhanced to aid in observation of the thin whisker)

Effects of Storage Temperature:
Contrary to other studies on tin whisker formation, GSFC observed higher density of whisker growth on samples stored under room ambient conditions (approx. 22°C, 30%-70% RH) than on samples stored at 50°C. This is not at all unusual in the study of whiskers - experimenters often find conflicting results, suggesting there is some underlying factor or factors that are not recognized and are not being controlled. This situation makes it particularly difficult for us to have confidence in claims by commercial interests that they have developed whisker-free coatings, especially given the great variability in incubation time that is also reported in this literature. Table 1 provides a comparison of the whisker density and typical length after 2 years versus storage conditions and substrate preparation. These comparisons were made for whisker formations from non-conformal coated sides only.

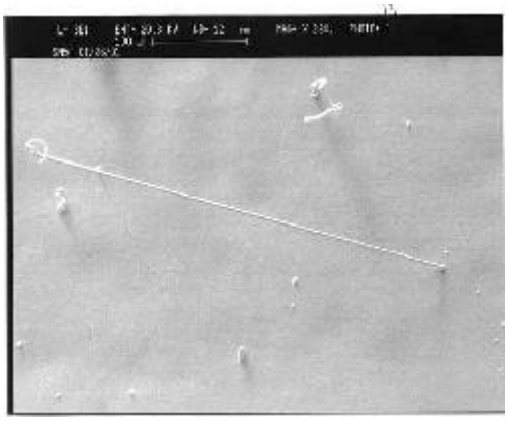
Table 1. Whisker density and length comparison between the specimen stored at 25 °C and 50 °C after 2 years.
(Non-Coated Specimens)

Stored at 50 °C					
Specimen without Cu flash			Specimen with Cu flash		
S/N	Average density (whiskers/mm^2)	Typical whisker length for needle-like whiskers (um)	S/N	Average density (whiskers/mm^2)	Typical whisker length for needle-like whiskers (um)
1T	18	20	1C	6	20
2T	18	20	2C	6	20
3T	18	20	3C	17	200
4T	18	20	4C	7	280

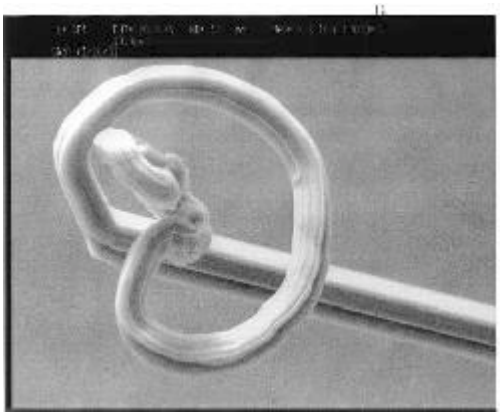
Stored at room ambient conditions					
Specimen without Cu flash			Specimen with Cu flash		
S/N	Average density (whiskers/mm^2)	Typical whisker length for needle-like whiskers (um)	S/N	Average density (whiskers/mm^2)	Typical whisker length for needle-like whiskers (um)
5T	50	900	5C	26	250
6T	50	900	6C	32	138
			7C	32	132

As shown in Table 1, the density of the whiskers on samples stored at room temperature is two to three times higher than for those stored at 50°C. This observation is independent of the presence of a copper flash intermediate layer between the brass substrate and the tin plating. In general, the whiskers are also much longer on specimens stored at room temperature. This finding contradicts observations reported by other experimenters. The longest whisker we have observed to date is about 2 mm long after just over 2 years

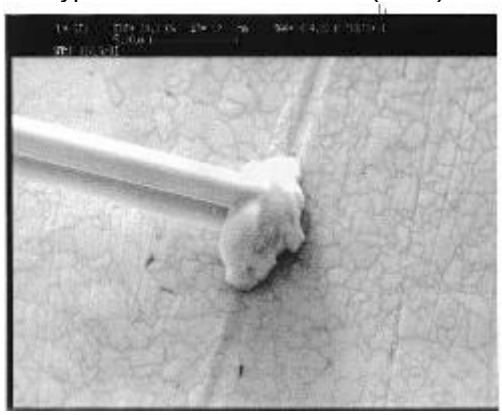
Some photographs documenting growth behaviors of tin whiskers on non-conformally coated specimens are shown in Figure 5.



A. Typical needle-like whisker (x230)

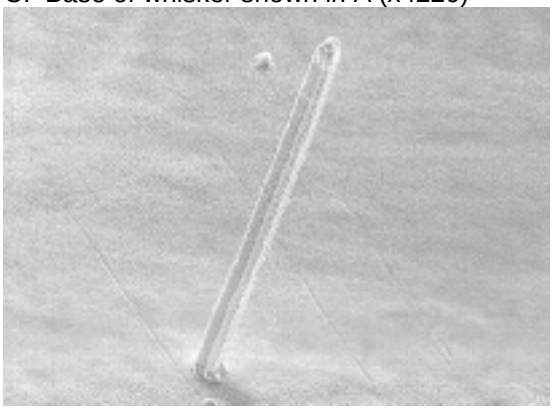


B. Tip of a whisker shown in A. (x3200)

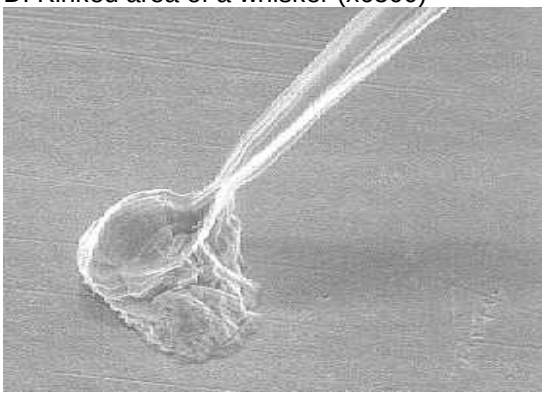


C. Base of whisker shown in A (x4220)

D. Kinked area of a whisker (x6500)



E. Typical straight whisker (x450)



F. Thinning of a whisker (x2200)

Figure 5. Various tin whisker formations observed in GSFC experiments

Conclusions

Catastrophic failures of electronic systems caused by tin whisker induced short circuits have been reported in commercial satellite applications. Despite decades of research into the tin whisker phenomenon, a comprehensive understanding of the mechanisms that affect their growth is not available. Currently, there are no industry accepted test methods for determining a particular component's (or plating process's) propensity to form tin whiskers. Some experimenters report the incubation time before initiation of whisker growth can be months, if not years. These observations are particularly concerning for long duration missions.

Historically, various forms of pure tin plating (especially, "bright" tin plating) have been found to be prone to tin whisker formation. Currently, the most effective risk mitigation technique against tin whiskers is to avoid the use of components that are most prone to whiskering of the form that is large enough to pose a reliability hazard. In the event such usage cannot be avoided or confirmed, users are advised to carefully review the use of pure tin plated components against application conditions, circuit geometries and mission objectives.

NASA GSFC is evaluating the effects of Uralane 5750 on tin whisker formation. Experimental observations and data are summarized below:

1. Uralane 5750 does not prevent whisker formation
2. Uralane 5750 shortens the incubation period of whisker formation
3. Although, whiskers initiate more rapidly under Uralane 5750, the coating also retards the growth rate of whiskers
4. Whiskers are capable of growing out from beneath a 1/4 mil thick Uralane 5750 coating
5. Tin whiskers can bend under forces of electrostatic attraction, thus increasing the probability of shorting

NASA GSFC is continuing this evaluation and plans to perform periodic inspections of the test specimens to further document the effectiveness of the conformal coat against tin whisker induced problems. In addition, GSFC is planning to evaluate some of the following issues:

- Tin whisker growth from pure tin plated capacitor terminations
- Tin whisker growth from pure tin plated leads of Plastic Encapsulated Microcircuits (PEMs)
- Tin whisker growth from pure tin plated shell of connectors
- Tin whisker growth from Tin/Lead finished components
- Evaluation of conditions that may accelerate tin whisker growth in conjunction with an industry task group trying to develop test methods to quantify whisker propensity of various plating chemistries.

This work is being done under the guidance of Dr. Henning Leidecker and Mike Sampson at NASA GSFC.

References:

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3 J. Brusse, “Tin Whiskers: Revisiting an Old Problem”, EEE Links, Vol. 4, No. 4, pp. 5 – 7, December 1998.
4 H. Leidecker, and J.S. Kadesch, "Effects of Uralane Conformal Coating on Tin Whisker Growth", Proceedings of IMAPS Nordic, The 37th IMAPS Nordic Annual Conference, pp. 108-116, September, 10-13, 2000.
5 Boeing Satellite Systems (formerly known as "Hughes Space") Website: http://www.hughespace.com/hsc_pressreleases/98_08_11_601ok.html
6 D.H. Van Westerhuyzen, P.G. Backes, J.F. Linder, S.C. Merrell and R.L. Poeschel, "Tin Whisker Induced Failure in Vacuum," 18th International Symposium for Testing & Failure Analysis, pp.407 - 412, October 17, 1992.
7 J.H. Richardson, and B.R. Lasley, "Tin Whisker Initiated Vacuum Metal Arcing in Spacecraft Electronics," 1992 Government Microcircuit Applications Conference, Vol. XVIII, pp. 119 - 122, November 10 - 12, 1992.
8 Satellite Outages and Failure Website: http://sat-nd.com/failures/hs601.html

Joint Airlock Enhances International Space Station Spacewalk Capabilities

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Space Shuttle Mission STS-104, launched on July 12, delivered the Joint Airlock to the International Space Station (ISS). Prior to delivery of the Joint Airlock, extravehicular activity (EV's) were conducted from the Space Shuttle Orbiter airlock and were, therefore, restricted to its presence. During the STS-104 mission, the crew installed, activated, and performed the first EVA from the Joint Airlock. The Airlock provides the on-orbit crew continuous EVA capability in both NASA Extravehicular Mobility Unit's (spacesuits) and in Russian Orlan spacesuits.

ISS Expedition 2 crew member, Susan Voss, used the Space Station robot arm (Canadarm2) to lift the Airlock from the shuttle payload bay and install it on the Unity Module of ISS. When used to conduct an EVA, the airlock recovers over 90 percent of the gases that were previously lost when airlocks were vented to the vacuum of space. Two system racks and two storage racks outfit the interior of the airlock, and it has a total pressurized volume of approximately 950 cubic feet.

Also delivered to orbit by this flight are four High Pressure Gas Tanks, two oxygen and two nitrogen. These pressure vessels were installed on the exterior of the Airlock during an EVA. Each tank is installed separately and is capable of recharge on-orbit. The tanks support EVA operations and augment the Service Module gas resupply system.

Figure 1: US Airlock prior to launch in the Space Station Processing Facility at Kennedy Space Center, Florida

Figure 2: One of the four high pressure gas tanks which will be mounted on the exterior of the Joint Airlock to support EVA operations.

Preliminary Evaluation of Data Retention Characteristics for Ferroelectric Random Access Memories (FRAMs)

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1.0 Introduction

1.1 FRAM Technology Background

Ferroelectric memory (FRAM) is a RAM-based device that uses the ferroelectric effect as the charge storage mechanism, and is very different from the floating-gate based nonvolatile memories. The ferroelectric effect is the ability of material to store an electric polarization in the absence of an applied electric field. A FRAM memory cell is fabricated by depositing a film of ferroelectric material in crystal form between two electrode plates to form a capacitor, which is very similar to a DRAM capacitor. However, instead of storing data as charge on a capacitor like a DRAM, a ferroelectric memory stores data within a crystalline structure. The Petrovskite crystals of the ferroelectric material maintain two stable polarization states resulting from the alignment of internal dipoles, corresponding to states of logical "1" and "0". The application of an electric field that exceeds the coercive field of the material will cause this alignment, while the reversal of the field reverses the alignment of these internal dipoles.

A simplified model of a ferroelectric crystal is shown in Figure 1(a) [1]. It has a mobile ion in the center of the crystal, and applying an electric field across the face of the crystal causes this ion to move in the direction of the field. A reversal of the field causes the ion to move in the opposite direction. The ion position at the top and bottom of the crystal are stable, and the ion remains in these states when the external field is removed. Since no external electric field or current is required for the ferroelectric material to remain polarized in either state, a memory device can be built for storing digital (binary) data that will not require power to retain information stored within it. Typical perovskite ferrolelectric materials are $BaTiO_3$, $PbTiO_3$, PZT($PbZr_{1-x}$ Ti_xO_3), PLZT($Pb_{1-x}L_xZrO_3$), PMN($PbMg_{1-x}Nb_xO_3$), SBT($SrBi_2Ta_2O_9$), SBN($SrBi_2Nb_2O_9$), etc [2].

Figure 1(b) shows a typical hysteresis curve of a ferroelectric capacitor and the response of the polarization (P) to the externally applied electric field (E).

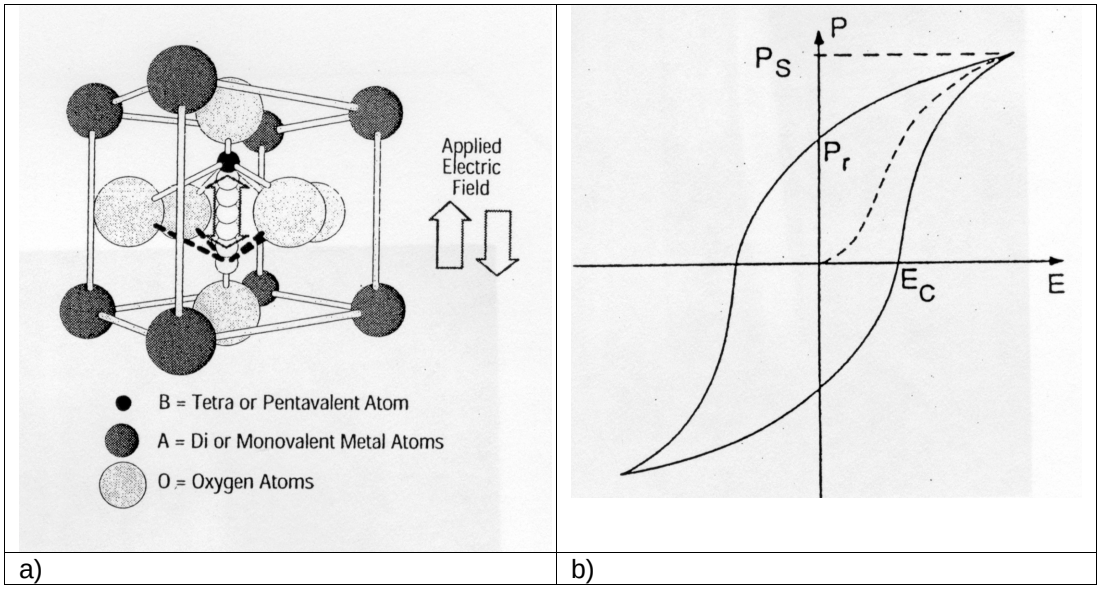

Figure 1. A ferroelectric material (a) Perovskite crystal unit cell, and (b) Typical hysteresis curve

1.2. FRAM Reliability Issues

Data retention, which is defined as the ability to maintain stored data between the time of writing and subsequent reading of the stored information, is one of the most important characteristics of the non-volatile memory devices. Retention failures, as well as failures due to the time dependent dielectric breakdown and leakage currents in memory cells are known failure mechanisms in all non-volatile memory devices, including FRAMs.

Test data on low density Ramtron FRAMs has demonstrated the failure rate of less than 60 fits with a 60% confidence level for 10-year data storage at room temperature [3]. However, the retention characteristics depends on multiple manufacturing and design factors and remain a major concern for reliability evaluation of new generations of FRAMs. Temperature, significantly accelerates retention failures due to thermal depolarization of the poled state in the ferroelectric material. In addition to retention failures, there are other failure modes and mechanisms that are specific to ferroelectric memory cells such as fatigue, aging, imprint, failures caused by reducing-environment conditions and radiation.

The major objective of this task was to evaluate reliability of FRAMs (with a focus on data retention characteristics) for their potential usage in space applications.

2.0 Part Description

Fifty FRAMs in ceramic 28-DIP packages (FM1608S-250CC) and fifty microcircuits in 28-DIP plastic packages (FM1608-P) manufactured by Ramtron were used for this evaluation. The FM1608 is a 64 Kbit, nonvolatile memory; organized as 8,192 x 8 bits that uses an advanced ferroelectric process. Functional operation of the FRAM device is similar to an SRAM. The users can access 8,192 memory locations, each with 8 bits through a parallel interface. The complete address of 13-bits specifies each of the 8,192 bytes uniquely. Internally, the memory array is organized into 8 blocks of 1 Kb each. The three most significant address lines decode one-of-eight blocks. Figure 2 shows the block diagram, pin description and functional truth table for the FM1608.

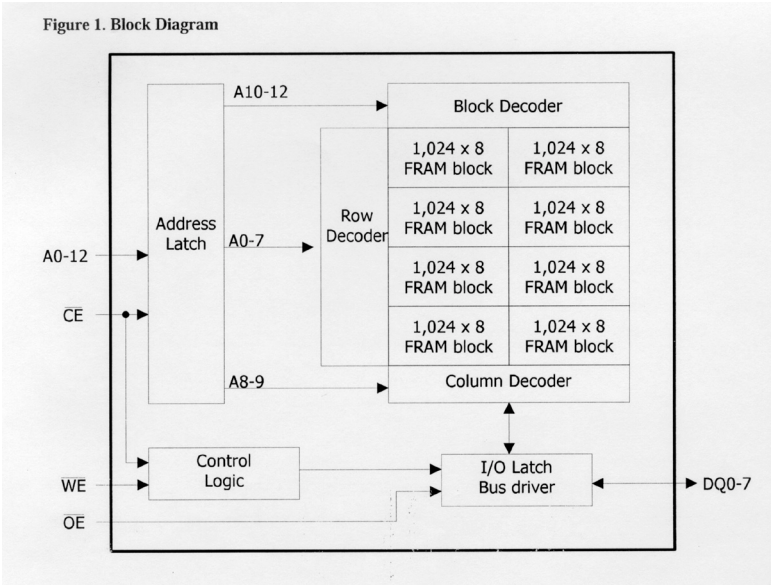

Figure 2. FM1608 Block diagram.

3.0 Test Description

A total of 100 parts, 50 each of ceramic 28-pin DIPs and plastic 28-pin DIPs were divided into various groups and subjected to high temperature storage aging tests at 150 °C, 175 °C, 200 °C*, 225 °C*, 250 °C*, and 275 °C* (* ceramic packages only) for several thousand hours cumulative, with interim and final electrical measurements (EM) for each lot. A high temperature, step-stress test was performed to estimate the temperature range, which causes high rate of retention failures. Low temperature exposure testing was performed on a lot of parts at – 85°C. Temperature cycling was performed between – 65°C and +150°C for 425 cycles with interim and final EM. In addition, extensive read-write cycling, and total dose ionizing radiation testing was also performed on some lots of parts.

Electrical measurements were performed using HP82000 digital tester and included parametric and functional measurements. The parametric measurements included input and output voltages and leakage currents (VOL, VOH, IIL, IIH, ILO_L, ILO_H), stand-by and active power supply currents (ICCSB_cmos, ICCSB_ttl, ICCOP) and

chip enable access time (tCE). During the functional testing, six data patterns ("scan 1", "scan 0", "check error board" and three pseudo-random patterns) were consequently written and then read for each test sample. The functional test frequency was 1 MHz.

To evaluate retention characteristics of the parts, each sample was subjected to parametric measurements and then to the functional testing with the pseudo-random pattern 1 (PRP1). Electrical measurements after the parts had been stressed for a specified period of time (retention period) at specified environmental conditions started with reading the PRP1 and followed by the parametric measurements. All parts passed initial characterization testing consisting of radiography and PIND testing, and then were preconditioned by 10,000 write-read cycles. No failures during preconditioning and/or initial electrical measurements were observed.

4.0 Temperature Dependence of Data Retention Time

Based on data obtained from high temperature aging test, a proportion of failed vectors was plotted with time on a Weibull probability chart (see Figure 3). The data can be approximated with two lines: a low-slope line ($\beta << 1$) at relatively low retention times and a high-slope line with $\beta > 1$ at large retention times. The low-retention-time failures are due partially to the intermittent failures, whereas the high-retention-time failures (high-beta lines) are due to "intrinsic" failures of the FRAM cells caused by a thermally activated loss of polarization. Extrapolation of the high-beta lines allows for estimation of the median time-to-failure for a vector. These data are plotted on the Arrhenius chart in Figure 4. It is seen, that the retention medium time-to-failure follows the Arrhenius law:

$$MTTF = A*\exp(E/kT)$$

with an activation energy E = 1.05 eV. Extrapolation to normal conditions shows that the MTTF for a vector exceeds 10^4 years at room temperature. The number of vectors in 64K FRAM is 8192, which corresponds to the MTTF of more than 280 years at room temperature.

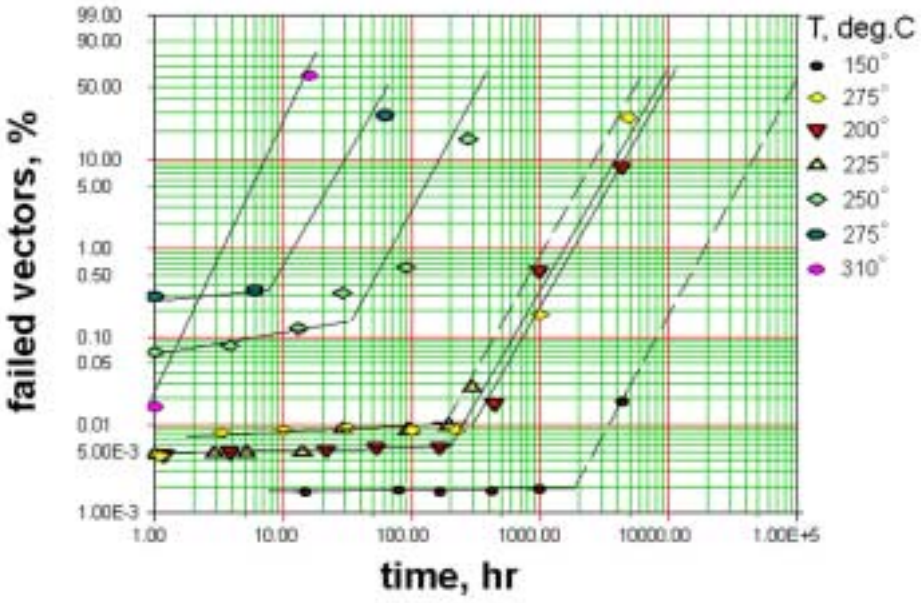

Figure 3. Cumulative proportion of failed vectors in ceramic parts.

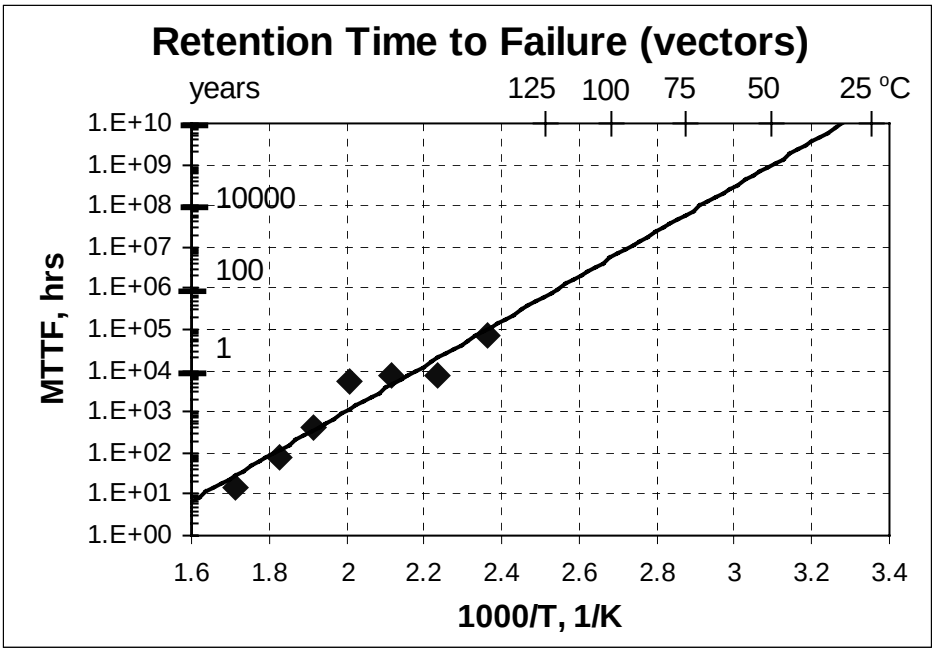

Figure 4. Temperature dependence of the medium time-to-failure.

5.0 Conclusions

Test results and conclusions are summarized below. For details, refer to complete report being posted on the NEPP web page.

1. Retention characteristics of 64k FRAM microcircuits were characterized in temperature range from -85°C to +310 °C during retention periods, up to several thousand hours with the following results:

1.1. No parametric or functional failures (when the reading immediately followed the writing) occurred during multiple ceramic and plastic parts testing at aging temperatures below 250 °C.

1.2. Observed retention test failures can be divided in three categories:

- Random failures, which are not related to stress conditions. Plastic parts had approximately 15 times higher probability of similar failures.
- Weak cell failures, which were also not related to a stress condition, but were reproducible from test to test. One-two failed vectors systematically appeared in some parts during the aging tests. Similar failures could be screened out by implementing a high temperature data retention test.
- Intrinsic failures, which were caused by a thermal degradation of the ferroelectric cells. Similar failures occurred in ceramic parts after tens or hundreds hours of aging at temperatures above 200 °C. An estimated activation energy of the retention test failures is approximately 1.05 eV, and the extrapolated mean time to failure at room temperature is more than 280 years.

1.3. No parametric or functional failures of ceramic or plastic parts were detected during multiple (up to 425 cycles) temperature cycling from –65 °C to +150 °C. Both type of parts (ceramic and plastic) withstood retention test with 285 temperature cycles between writing and reading.

1.4. Retention test at –85 °C did not reveal any intrinsic failures. However, some random failures occurred both in ceramic and in plastic parts. The long-term storage (more then 5000 hrs retention time) of the parts did not result in any parametric or functional degradation.

1.5. No retention, parametric, or functional failures occurred with ceramic parts during radiation tests (total dose 90 krad Si). Plastic parts had some random data retention test failures.

2. Operational current measurements with different patterns allow for estimation of the levels of switching and non-switching polarization in the ferroelectric cells. The difference between these two currents depends on the average remnant polarization and can be used for monitoring degradation processes in the memory

cells. However, additional analysis should be performed to reliably establish the relationship between the operational currents and the level of cell polarization.

3. Multiple write-read cycling (up to $3x10^7$) during fatigue testing of the plastic and ceramic parts did not result in any parametric of functional failures. However, operational currents linearly decreased with the logarithm of number of cycles, thus indicating fatigue process in the PZT films. This process was accompanied with approximately 20% decrease of the data access time in ceramic parts. Plastic parts manifested significantly smaller changes in operational currents and data access times, which could be due to the different die lot (improved process) used in manufacturing of these parts.

4. Test results confirmed that the PZT-based FRAM microcircuits potentially may have very high data retention and virtually fatigue-free characteristics over a wide interval of temperatures and write-read cycles. This, as well as a high radiation tolerance makes this devices an attractive technology for space applications. However, further improvements in the manufacturing process and/or testing and screening systems are necessary to detect and eliminate devices susceptible to random soft failures.

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Thermal Cycling/Shock Behavior of CSP Assemblies

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Abstract

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. The experience of the Consortium in building more than 150 test vehicle assemblies, single- and double-sided multilayer PWBs, and the environmental test results has now been published as a chip scale package (CSP)guidelines document and distributed by Interconnection Technology Research Institute (ITRI).

The Consortium assembled fifteen different packages with I/Os from 48 to 784 and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). Another test vehicle was designed and assembled by a team member using their internal resources and was identified as TV-H. The TV-H assemblies were subjected to numerous thermal cycling conditions including -55°C to 125°C with two ramp rates, one thermal cycle with 2° to 5°C/min and the other near thermal shock. Cycles-to-failure (CTF) test results to 1,000 cycles and 400 cycles under these conditions are presented for 180 and 208 I/O fine pitch ball grid arrays (FPBGAs) with three die sizes. Decrease in CTFs due to ramp rate and die size increase for different I/O FPBGAs with 0.8 mm pitch are compared and analyzed.

Introduction

Chip scale packages are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refers to a package with a pitch of 0.8 mm and lower. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when they are assembled onto boards. A test vehicle (TV-1) with eleven package types and pitches was built and tested by the JPL MicrotypeBGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guidelines document for industry use[1].

The finer pitch CSP packages which subsequent to TV-1 became available were included in a follow-on test vehicle of the JPL CSP Consortium [2]. The Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables.

One test vehicle, herein refers to TV-H, was designed and assembled by Hughes Network System using their internal resources. This paper presents the thermal cycling test results to 1,000 cycles (-55 to 125°C) for a variety of CSPs used on the TV-H assembly. CTF test results are compared to those performed under this temperature range, but with a more severe near thermal shock condition to 400 cycles.

TEST MATRIX

Test Vehicle Package I/O /PWB

The TV-H had eight packages with I/Os ranging from 48 to 280 and pitches of 0.8 mm to 1mm. The PWB had four layers with the two resin coated copper (RCC) layers and an FR-4 core (1+2+1) having a total thickness of 0.43 mm. Microvia technology was used. The pad had a 0.1 mm (4 mil) microvia hole at the center of pad. A non-solder-mask-design (NSMD) pad with a diameter of 0.3 mm and 0.05 mm clearance was used. The surface finish of the PWB was Ni/Au immersion with about 2-8 micro inch of gold over 100-200 micro inch Ni. No clean solder paste was applied for assembly using a 5 mm laser-cut stencil thickness. The test vehicle was 11.9 cm by 4.6 cm (4.75″ by 1.85″) with a connector interface for continuous monitoring of daisy chains during thermal cycling.

Test Vehicle Features/Daisy Chain Patterns

A full populated test vehicle (TV-H) with two sites for the 280 I/O fine pitch ball grid array (U4 and U2 sites) was shown in the January 2001 issue of EEE Links. All packages were daisy-chained, and they were divided into several internal chain patterns. The daisy chain pattern on the PWB completes the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic testing. All packages were prebaked at 125°C for 2 ½ hours prior to assembly.

TEST CONDITIONS

Thermal Cycling test

Thermal cycling was performed in the range of -55°C to 125°C under two different conditions. Chamber setting and thermal couple readings for conditions A and B are shown in Figure 1 and 2, respectively. For condition A, the heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes.

The near thermal shock cycle, condition B, had the same temperature range performed in a chamber with three regions of hot, ambient, and cold. Heating and cooling rates were nonlinear and varied averaging between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

Monitoring

The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 7.8, were used as guidelines to interpret electrical interruptions. In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. This was not the case especially for the wafer level package assemblies. Failures detected by continuous monitoring were verified manually at room temperature after weekly removal from the chamber.

THERMAL CYCLING RESULTS

Figure 3 shows the test results for the 180 I/O FPBGA with a die size of 6.3 mm and the 208 I/O with the die sizes of 11.4 and 9.5 under the same thermal cycling range (-55°C/125°C), but with two different ramp rates, A and B conditions. It is apparent that under the near thermal shock cycle, the CTFs for the 208 I/O package with 11.4 and 9.5 mm dies were within the data scatter. This is not the case for those under thermal cycle A condition where the effect of die size clearly demonstrated. The CTFs for the 180 I/O package with a 6.3mm die size are also differed significantly under two cycling conditions. The CTFs were in the range of 145 to 389 cycles for the near thermal shock whereas the first failure was observed at 778 cycles for the thermal cycle condition.

CONCLUSIONS

These conclusions are based on the results limited to assembly failures to 1,000 thermal and 400 near shock cycles in the range of -55°C to 125°C. Addition thermal and mechanical cycling data with their failure analyses are being gathered to further define the effects of various parameters on assembly reliability.

- Cycles-to-failures for the fine pitch ball grid arrays (FPBGAs) with 0.8 mm pitch were in the range of 300 to 800 and 100 to 200 cycles for thermal cycle and near thermal shock conditions, respectively. The CTFs fir both conditions are significantly lower than the ones observed earlier with their 1.27 mm pitch BGA counterparts [1].
- CTFs decreased as package die size increased under thermal cycle condition. The effect of die size decrease from 11.4 mm to 9.5 mm could not be clearly identified by the near thermal shock condition. Additional tests are being performed for further analysis.
- The 208 I/O FPBGA package with the largest relative die size to package dimension (11.4 mm die in 15x15 mm package) showed the lowest CTFs and the 180 I/O package with the lowest relative die size to package (6.3 mm die in 12x12 mm package) showed the highest CTFs under thermal cycle condition.

Acknowledgments

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We express our special thanks to Dr. Namsoo Kim at Boeing for his technical leadership support, M. Chisa and Kevin Griffith, and A. Arreola (JPL) for leading monitoring the environmental testing. The author also would like to acknowledge the in-kind contributions and cooperative efforts of the JPL CSP Consortium.

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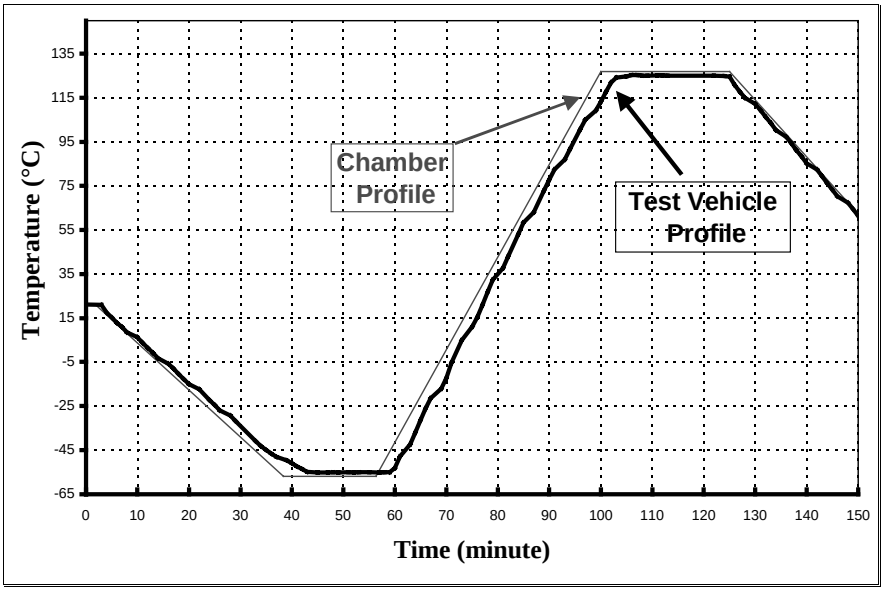

Figure 1: Thermal cycle profile in the range of –55°C to 125°C, condition A, 159 minutes/cycle

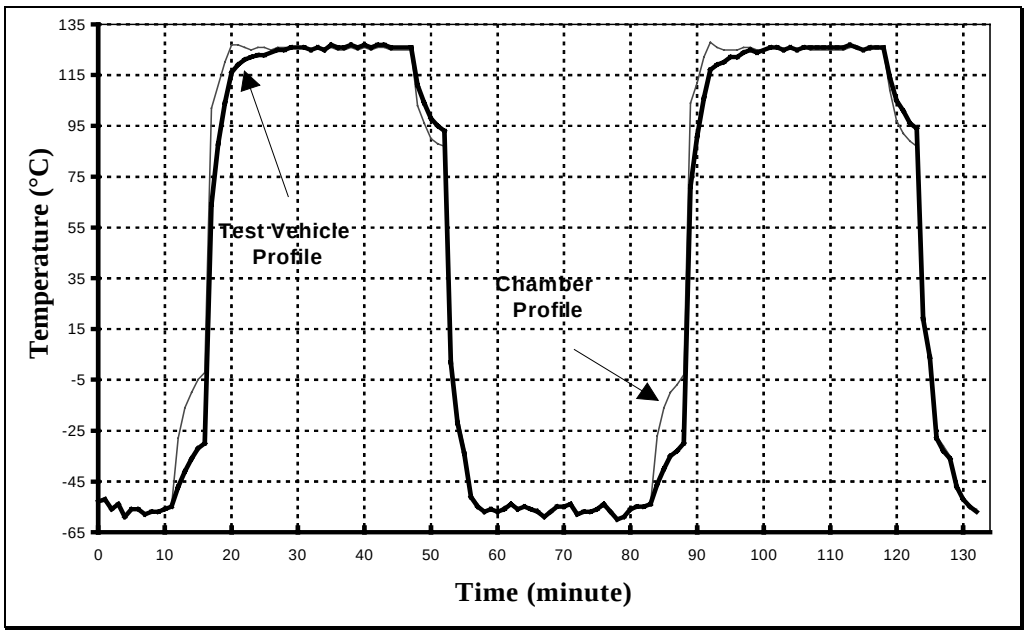

Figure 2: Near thermal shock profile in the range of –55°C to 125°C, condition B, 68 minutes/cycle

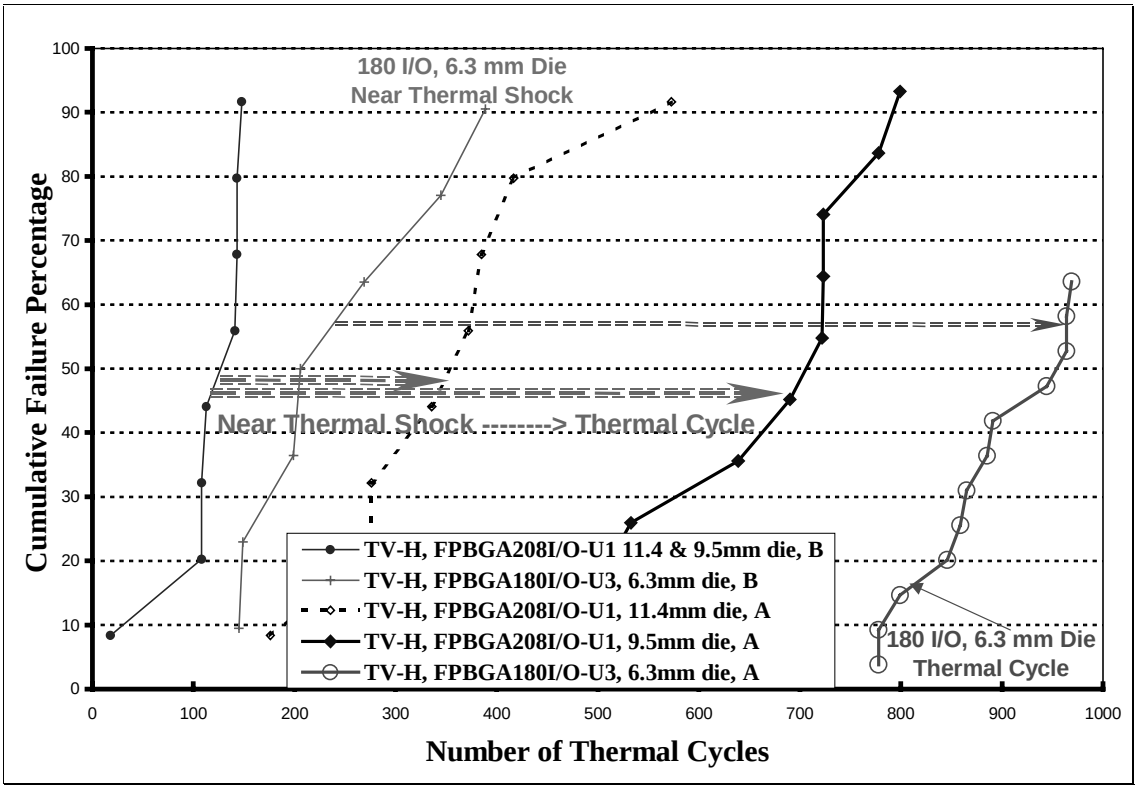

Figure 3: Cumulative Failure Distribution for the Same FPBGA Package and I/Os Under the Same Thermal Cycling Range (-55 ° to 125°C) But Two Different Rates

Evaluation of Maxwell Technology PowerCache Ultracapacitor

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Introduction

The Parts Analysis and Assurance (PA&A) group at the Johnson Space Center (JSC) evaluated the PowerCache Ultracapacitor, part number PC5, from Maxwell Technology. These capacitors are used in the ISS PEEK (Portable Electrical Equipment Kit). The PEEK hardware provides electrical power extension cables and outlets as well as 120 to 28Vdc converter units to power portable electrical hardware on the ISS.

Ultracapacitors, also known as double-layer capacitors, incorporate new technology and material not used in other capacitors. The ultracapacitor stores electrostatic energy by polarizing the electrolytic solution and can be charged and discharged hundreds of thousands of times. An electrode-electrolyte interface with activated carbon fibers allows obtaining extremely high capacitance per unit area. There are several methods of construction, but JSC tested one where an insulator separates two activated carbon electrodes. These electrodes consist of an aluminum foil with a carbon binder mixture deposited in it. The set is tightly rolled with leads attached to the aluminum foils. An electrolyte is added and the component is sealed.

This technology is suited for applications where there is a need of providing large bursts of power, for fractions of seconds up to several minutes, with the ability of rapid recharge. During a power outage, power levels from the ultracapacitor can be held until power returns. Due to their large energy storage capability, ultracapacitors have found applications in the electric vehicle industry, memory back-up devices in appliances such as videocassette recorders, typewriters, wristwatches, and measuring devices. The advantage of ultracapacitors is that they are smaller in size than other capacitors of the same value. This allows for greater packaging efficiency. The typical voltage rating for a single ultracapacitor is 2.3Vdc. The components can be stacked in series to achieve the proper operating voltage for any specific application.

Space Application

The PEEK project had the JSC RITF (Receiving and Inspection Test Facility) evaluate these commercial capacitors to determine their suitability in space flight hardware. The evaluation consisted of a series of tests to determine their performance across a range of environmental stress conditions. The following tests were conducted:

- Visual Inspection
- Fine Leak Test
- Accelerated Life (Six tests)
- Static Burn-in (five tests)
- Reverse Bias
- Self-Heat via Rapid Charge-Discharge (three tests)
- Over Voltage Pulse (eleven tests)
- Thermal Shock (one test)
- Destructive Physical Analysis
- Electrical Parameter testing at periodic intervals

The RITF test results demonstrate that the ultracapacitor is suitable for use in the ISS PEEK hardware, as well as in other equipment that is used in ISS manned pressurized modules. Ultracapacitor pedigree in military or aerospace applications is presently not available and no specific standard has been developed for screening and testing purposes. However, the PowerCache ultracapacitor survived the environmental tests in MIL-STD-810 “Environmental Engineering Considerations and Laboratory Tests”. A series of tests were performed at JSC Receiving Inspection and Test Facility (RITF) to determine the reliability of the ultracapacitor under different conditions. The PC5 ultracapacitor is rated at 4 Farads at 2.7Vdc maximum and the operating temperature is between -20ºC to +70ºC.

Investigation

Fifteen ultracapacitors were tested, all receiving the fine leak test and visual inspection. The ultracapacitors are hermetically sealed; therefore, the fine leak test was performed in accordance with MIL-STD-883 test method 1014 during initial inspection and at the completion of all tests. The ultracapacitors did not exceed the leakage limit imposed by the test method.

The ultracapacitors were divided into groups of five and ten. Ten ultracapacitors received accelerated life tests, which consisted of six dynamic tests. The ultracapacitors were charged-discharged cycled 6000 times, at three different temperatures (-20ºC, +25ºC and 65ºC). They were first cycled 1000 times and then 5000 times. The charge voltage was 2.3V and each cycle was approximately 1.5 minutes in duration. They were subjected to a total of 18000 cycles. The monitored parameters (C, ESR, and LC) did not change significantly as a result of these tests.

A total of 480 hours of static burn-in while charged at 2.5V was performed on the ten ultracapacitors. The burn-in consisted of 96 hours at +60ºC, 48 hours at –20ºC, 48 hours at –5ºC, 48 hours at 0ºC and 240 hours at +85ºC. The 240 hours of burn-in resulted in a change in capacitance, ESR and LC. However, the parameters remained within the manufacturer's specification.

For the reverse bias test 5 ultracapacitors were connected in reverse polarity. They operated this way for 5000 charge-discharge cycles at 65ºC. The duration of the cycles was approximately 1.5 minutes in duration. After 5000 cycles, the capacitance of the 5 ultracapacitors was reduced to almost half and the ESR almost tripled.

Ten ultracapacitors were subjected to 100 cycles of thermal shock between –55ºC to 85ºC. The ultracapacitors were not connected to any circuit or power for this test. No significant change in the parameters resulted at the completion of the test.

Two ultracapacitors were tested for self-heat via rapid charge-discharge. The test consisted of charge-discharge at a rate fast enough to cause internal heating. When the desired temperature was reached, the ultracapacitors continued to be cycled for five minutes at that temperature. No significant change in the parameters resulted from the test.

Two ultracapacitors were subjected to over voltage pulse test. The test consisted of voltage pulses of varying amplitude and of varying duration. The test did not result in significant change in the parameters.

Destructive Physical Analysis (DPA) was performed in accordance to MIL-STD-1580 on a sample. The sample was a representation of the 15 ultracapacitors. The sample was examined externally and internally. No anomalies were found.

Conclusion

One test, the reverse bias test, caused damage to the ultracapacitor as expected. These are polarized devices and are not to be used in reverse polarity. In all the other tests, the ultracapacitors continue to work as advertised within the specification. The 240 hours of burn-in at 85ºC, resulted in drift of capacitance, ESR and LC. However, this change was never beyond the specification and the capacitor continued to work properly. Two of the tests designed to overstress the part, self-heat via rapid charge-discharge and the over voltage pulse, did not cause any damage.

The results of these tests show that the PowerCache ultracapacitor from Maxwell is highly reliable when used within the manufacturer's specification. The series of tests performed on the ultracapacitor showed the suitability of the device in the space flight crew compartment. The ultracapacitor demonstrated that it could operate beyond the manufacturer's operating parameters. However, care must be taken in the operating temperature. The ultracapacitor operating temperature is –20ºC to +70ºC but the space and military operating temperatures exceed this range.

CONDUCTING POLYMERS AND THE EVOLVING ELECTRONICS TECHNOLOGY

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INTRODUCTION. Polymers are generally known as insulators. In 1981, the U.S. produced more than 24 million metric tons of polymers, more than the volume of steel. Polymers are simply very large molecules (macromolecules) that are made up of smaller molecules (monomers) that can be linked together in various ways, resulting in a range of what we call microstructures (e.g. linear chains, branched chains, densely interconnected networks etc.). Plastics that conduct electricity have been around since 1970's, but their electronic properties, and widespread use, have been limited by structural disorder. Polymers are a shiny material derived from acetylene, whose electrical conductivity surpassed those of conductors. The oxidation of Polyacetelene with Iodine, using Ziegler-Natta-catalyst yielded this material. H. Shirakawa, A.G. MacDiarmid, and A. J. Heeger shared the 2000 Nobel Prize for Chemistry, for the discovery of Conducting Polymers. This new technology is being used in anti-static and anti-corrosive materials, electronic integrated circuits, photonics, displays, lasers, sensors, photovoltaics, actuators, and electromagnetic shielding. Compared to silicon technology, polymers are not only flexible, but cost less to manufacture.

The most promising materials are conjugated organic polymers, which are molecules with a "back bone" of alternating double and single bonds, along which electrons can flow. The simplest of these polymers is polyacetelene. The mechanical flexibility and tunable optical properties of some conducting polymers make them attractive materials for new optical and electronic devices, such as light emitting displays and biomolecular sensors. The properties of polymers used in emerging technology are: conductance, hydrophillic/hydrophobic state of the surface, color, volume, and permeability for gases/ions. Altering the specific chemical structure of intrinsically conducting polymers, (i.e. doping through oxidation or reduction processes) can vary conductivity.

Conducting polymers or synthetic metal oxidation introduces positive (+) charge carriers in the material and negative (-) ions in between these chains. Reduction produces the opposite effect. Intrinsically, conducting polymers were first discovered in 1977, as reported by C. K.Chiang et al. in Phys. Rev. Lett. 39, p. 1098 (1977). Since that time many more were discovered, but they could not be processed, nor were they air-stable. Now, we know of several conducting polymers that are air-stable and can be processed.

There are four types of semi-conducting polymers: (1) filled polymers with carbon black, graphite and metal particles, (2) ionically conducting polymers, (3) charge transfer polymers, and (4) conjugated conducting polymers.

I. Filled polymers are polymers loaded with conductive fillers such as carbon black, graphite fiber, metal particles or metal oxide particles.
II. Ionically conducting polymers are also called ionomers or polymer electrolytes. They have a wide range of commercial electronic applications, including rechargeable batteries, fuel cells and polymer light-emitting devices.
III. Charge transfer polymers have become the most established semi-conducting organic systems because of their commercial use in xerographic photocopiers. Most charge transfer polymers, including trinitrofluorenone doped poly(vinyl carbozole or PVK), triarylamine doped polycarbonate, and polysilanes are p-type materials. Although n-type materials have been reported, the electron mobility in such polymers is about three orders of magnitude lower than p-type materials.
IV. Conducting conjugated and charge transport polymers are the two important classes in semi-conducting organics. In conjugated polymers, polyaniline and modified polyaniline are being used as conductive fillers to give conducting filled polymers. Conducting polymers have bright light, they are cheap, flexible, easy to manufacture, and are sometimes better conductors.

The process of doping and de-doping is reversible. Due to this process, the intrinsically conducting polymers can easily be switched. They can go from the conducting to insulating state, from a permeable to non-permeable state, and range from red to blue in color [e.g. polyaniline (PAn) and poly (3-n-hexylthiophene)]. Polyaniline exists in a variety of oxidation and protonation forms. The various reaction conditions can lead to products with widely varying chemical, macromolecular and supramolecular structures.

APPLICATIONS:

The new devices made of conducting polymers are going to be used in every phase of life on earth, as well as in space Compared to other existing technologies, conducting polymers are lightweight, take up less space, and are less expensive to manufacture. They are also flexible, and in many cases unbreakable. These characteristics make them excellent for use in space vehicles, for human or robotic exploration and satellites. For example, the flexible and lightweight nature of these devices would be suitable to introduce built-in computers in space suits, with associated sensors to monitor the health of astronauts while they perform extra-vehicular activities. These devices could also be beneficial for tele-medicine in space due to their flexible nature that can follow the contours of the body. Conducting Polymer actuators are also being explored to be used in micro-robots, for un-manned space missions utilizing micro-satellites. To further qualify these devices for use in the harsh environment of space, more testing is needed to determine reliability, with regard to ionizing radiation, Solar UV, and extreme temperatures.

Currently, the benefits of these new devices are being used in a variety of parts in Commercial-Off-the-Shelf (COTS) equipment. Below is a list of some of the applications.

- Photonics (organic light emitting diodes, lap-top and TV displays, photo-diodes, and image sensors).
- Energy related equipment (fuel cells, flexible solar cells, improved energy density storage batteries, and super capacitors, etc.).
- Sensors (flow injection, electric field, pressure, voltage, light, stress, temperature, humidity, gas, odor and hazardous chemicals).
- Materials (gels, thermoplastics, composites).
- Electronic devices and integrated circuits (silicon hybrid thin film transistor, FETs, nano-FETs, electro-chromic devices, high current switches, and flexible printed circuit boards).
- Computing and information technology (storage, neural networks, optical signal processing, etc.).
- Medical Field (flexible vital sign and toxin sensors).
- Flexible light sources, as well as display devices.
- Lasers and electro-optics (electrically driven lasers and laser arrays, etc.).

Reliability Evaluation of MIT/LL FDSOI 0.25 μm Process for Space Applications (Part II)

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1.0 Introduction

The previous report titled, "Reliability Evaluation of Fully Depleted SOI (FDSOI) Technology for Space Applications," posted on the NEPP web site, provided a general overview of SOI technology including materials, process, reliability issues, and MIT/LL FDSOI processes and associated reliability test structures. The hot carrier degradation effects in the MIL/LL FDSOI FETs at $V_g = V_d/2$ conditions, which are known to maximize the interface trap generation have been investigated at JPL [1].

This report (Part II) of the continuing evaluation, addresses characterization of the N- and P-channel transistors, including scaling effects and estimation of the reproducibility of the front- and back-channel parameters was performed. The transistor measurements included threshold voltage, subthreshold slope, mobility of charge carriers, gate leakage currents, and investigation of the edge effects. Radiation effects and charge instability in FD SOIFETs will be discussed in part III of the report.

2.0 FDSOI Process Monitor Transistors

A detailed description of the test structures used in MIT/LL to control manufacturing process and, in particular, FDSOI FETs was provided in the previous report [2]. For this evaluation, four process monitor dice were received, containing NMOS/PMOS transistors of various sizes. There were 40 FETs in each dice with L = 0.2 μm to 0.8 μ and W = 0.5 μm to 100 μm.

The transistor structures were mesa-isolated and fabricated in SIMOX (separation by implantation of oxygen) wafers with silicon thickness 47 nm. The thickness of buried and thermal oxides was 170 nm and 7.3 nm. Polysilicon gates (200 nm of thickness) and active areas of the transistors were silicided after spacer formation.

3.0 FDSOI PM Parametric Measurements

The process monitor transistor characteristics were measured under probes using a Hewlett Packard Precision Semiconductor Analyzer (Model 4156A). Due to a strong coupling effect, characteristics of the front-channel transistors strongly depend on the voltage applied to the back gate and vice versa.

To characterize the gate oxide SOI and buried oxide SOI interfaces separately, the measurements were performed at "decoupling conditions" by biasing the opposite gate to create accumulation in the corresponding channel. The front gate characteristics were measured at +10 V on the back gate for N-channel transistors and –10V for the P-channel transistors. The back gate characteristics were measured at ± 1 V correspondingly for N- and P-channel transistors.

The threshold voltage, V_{th}, was measured using two methods: at the constant current level ($I_d = I_{th} = W/L*0.1$ μA at $V_d = 50$ mV), and in the ohmic region by $I_d/SQRT(g_m)$ extrapolation (where g_m is the transconductance) to the intercept with the horizontal axis. The subthreshold slope (S) typically was measured at the drain current range from
10^{-11} A to 10^{-8} A. The mobility of the carriers (μ) was calculated by measurements of the slope (K) of the $Id/SQRT(g_m)$ function in the ohmic region [3]-[4]:

$$\frac{I_d}{\sqrt{g_m}} = K(V_G - V_{th}), \qquad \ldots(1)$$

where $K = \sqrt{\frac{\mu V_d C_{ox} W}{L}}$ …(2)

The measurement included threshold voltage, subthreshold slope, mobility of the charge carriers, effective dimensions, gate leakage current, and investigation of edge effects- as briefly described below. For detailed test results and data plots, refer to full report being posted on the NEPP web site.

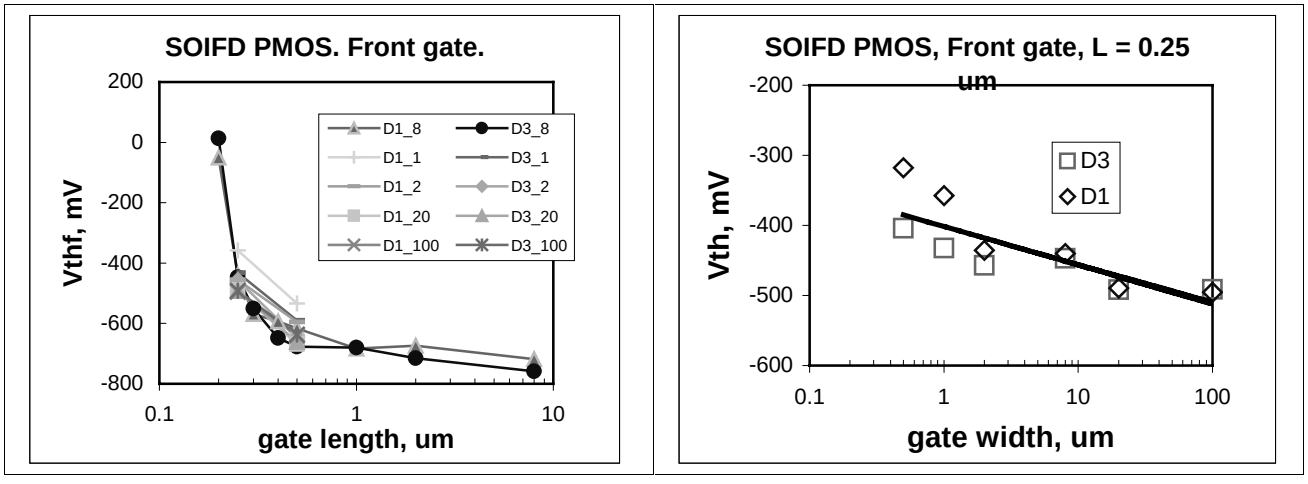
3.1 Threshold Voltage

The threshold measurements were made on 15 to 20 transistors of N- and P-type on three dice. Average and standard deviations of the V_{th} values for transistors with the same gate width and length were calculated. Mean value of these characteristics are shown in Table 1. It was observed that variation of the V_{th} within one wafer did not exceed 5% for the P-channel devices. However, characteristics of the front gate channels in the N-channel transistors were less reproducible and the variation reached 12%. The front-gate threshold voltage in P-channel transistors significantly increased with decreasing the channel length from approximately –850 mV at L = 8 μm to 0V at L = 0.2 μm. N-channel transistors manifested similar trend; however, the decrease was much smaller (on the average, from 550 to 420 mV) and scattering of the data was larger.

The scaling effect in SOI FD PMOS transistors is illustrated in Figure 1.

Table 1. Threshold Voltages of FDSOI FETs.

Gate	Mean V_{th}	Std. Dev.	Std. dev/avr, %
N-ch front	560.2 mV	65.8	11.7
N-ch back	8.3 V	0.5	5.7
P-ch front	-609.6 mV	23.2	4.4
P-ch back	-9.4 V	0.2	2.2



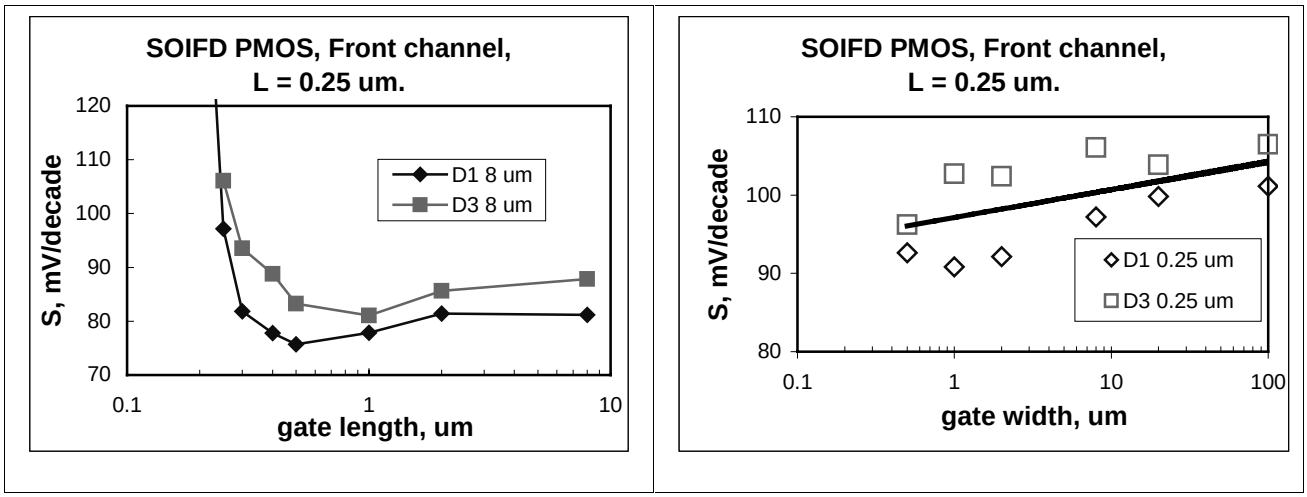


Figure1. Scaling Effects in FDSOI PMOS Transistors.

3.2 Subthreshold Slope

Average subthreshold slope values, their standard deviations, and variations from the calculated minimal values for 0.25 μm process transistors are shown in Table 2. It is seen that the variation of the S values is below ~ 10% except for the back channel in the NMOS transistors, where it reached ~ 20%.

Table 2. Subthreshold Slope (mV/decade)

Gate	average	Std.dev.	(S-Smin)/Smin, %
N-ch front	80	9	29
N-ch back	960	210	91
P-ch front	99	5	60
P-ch back	1110	98	120

3.3 Mobility of Charge Carriers

The front gate mobilities of the charge carriers in transistors of both types were approximately 20-30% less than the volume values, which is usually explained by additional scattering at the Si/SiO_2 interface. The back channel mobility was significantly larger than the front gate mobility.

3.4 Effective Dimensions

The calculations of the transconductnce parameter K (see Eq.2) for transistors with different drawn gate width (W_{mask})and length (L_{mask}) allows estimations of the effective channel length and width, which might deviate from the drawn values. The experimental data showed that in most cases, the gate size deviation from the drawn values is negligible.

3.5 Gate Leakage Current

Attempts to measure gate leakage currents directly showed that they were below the limit of HP4156 sensitivity ($<10^{-13}$ A in the used set up). For this reason, the gate lifting technique was used. The drain current was monitored after applying corresponding bias to contact pads of a transistor, following a mechanical disconnection (lifting) of the gate probe. The drain current decreased with time, indicating a decrease in the gate voltage caused by the oxide leakage current. The drain current declined exponentially and the characteristic time of the decay $\tau = RC$ (where R is the effective resistance of the oxide and C is the capacitance) allowed for calculation of the resistance. The calculations showed that the gate oxide resistance was approximately 2×10^{18} Ohm, which corresponds to negligible leakage currents in the range of femto-amperes

3.5 Edge Effect

A decrease in the gate width significantly increases the possibility that the parasitic conduction path between the drain and source at the lateral edges in SOI MOS FETs would provide a major contribution to the leakage current in the OFF condition of transistors. The side-wall transistor, which is always formed in mesa-isolated structures, operates in parallel with the main transistor and may cause failures of SOI devices.

Analysis of more than 100 different transistors performed in this work did not reveal any excessive leakage currents, which might be related to the edge effect, (except for one case where the current was approximately 10^{-11} A).

4.0 Conclusions

The front- and back-channel N-and P-type transistors manufactured in MIT/LL 0.25 μm SOIFD technology were fully characterized using three process monitor dice with 40 transistors in each die (the gate length varied from 0.2 μm to 8 μm and the gate width varied from 0.5 μm to 100 μm). The test results are summarized below.

- The variations in the threshold voltage and the subthreshold slope did not exceed 12% and 20 % (respectively for V_{th} and S). Characteristics of the front channels in NMOS FETs were much less reproducible than for the PMOS transistors.
- Both N- and P-channel transistors exhibited the short channel effect. The absolute values of the threshold voltage decreased significantly below 0.5 μm. The effect was most pronounced for PMOS transistors. A decrease in the gate width, also resulted in a decrease of the absolute value of the threshold voltage.
- The subthreshold slope also showed a strong gate-length dependence, significantly increasing in the submicrometer region (more than twice for the back channel, and approximately 15% - 25% for the front channel transistors).
- The mobility of the charge carriers virtually did not change with the gate length for the front-channel NMOS transistors and increased for the PMOS transistors when the gate length decreased below 0.5 μm.
- Electrical measurements showed that the gate length deviations did not exceed 2% of their drawn value.
- The specific resistance of the gate oxide was approximately 10^{15} Ohm*m and the gate leakage current was in the femto-ampere range.
- The parasitic side-wall transistor at the gate edge resulted in some deviations of the transconductance characteristics for the NMOS transistors with the gate width below 2 μm. However, no excessive leakage currents in the OFF condition of the transistors, or any other significant anomalies were observed.

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Optical Inspection of ADI OP Amp Packages Before and After Thermal Cyclying (-125°C to 90°C)

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Objective: The objective of this test is to evaluate the SOIC package of Analog Devices Operational Amplifier model OP 284 FS via thermal cycling tests and inspection by optical microscopy.

Introduction: This product has been proposed to use in the control electronics package of an actuator for Mars Exploration Rover Project. There could be some problems associated with the driver electronics package boards associated with the actuators that are available commercially under extreme environments. The board was redesigned and the new package will be built for MER. Therefore, parts group at JPL has undertaken an effort of upscreening the parts required to build such a package board. There are several parts in the package board. One of the parts is Analog Devices OP 284 FS. There are several steps involved in upscreening the plastic parts for any NASA project. Thermal cycling is one of the steps in upscreening the parts to choose the reliable parts to build the final board.

Features of OP 284 (Ref.: Website of Analog Devices): The features of this part are single supply operation, wide bandwidth (4 MHz), Low offset voltage (65 μV), unity gain stable, high slew rate (4 V/μs), and Low noise (3.9 nV/(Hz)$^{1/2}$). The OP184/OP284/OP484 are single, dual and quad single-supply, 4 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from +3 to +36 (or ±1.5 to ±18) volts and will function with a single supply as low as +1.5 volts. These amplifiers are superb for single supply applications requiring both ac and precision DC performance. The combination of bandwidth, low noise and precision makes the OP184/OP284/OP484 useful in a wide variety of applications, including filters and instrumentation. Other applications for these amplifiers include portable telecom equipment, power supply control and protection, and as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers. The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios. The OP184/OP284/OP484 are specified over the HOT extended industrial (-40°C to +125°C) temperature range. The single and dual are available in 8-pin plastic DIP plus SO surface mount packages. The quad OP484 is available in 14-pin plastic DIPs and 14-lead narrow-body SO packages.

Figure 1 shows the optical photographs of the ADI OP 284 that were taken before thermal cycling. Inspected the parts/packages (#621, 622, and 623) using optical microscopy and digital camera in the inspection laboratory of JPL.

Applications: Battery powered instrumentation, power supply control and protection, telecom, DAC output amplifier, and ADC input buffer etc. These parts may be used for space applications.

Package: The package type of this part is the standard 8-pin SOIC (Small Outline Integrated Circuit).

Absolute Maximum Ratings (Ref. Analog Devices Website):

Supply voltage =		±18 V
Input voltage =		±18 V
Differential input voltage =		±18 V
Storage temperature =		-65°C to 150°C
Operating temperature =		-40°C to 150°C
Junction temperature =		-65°C to 150°C
Lead temperature range (soldering 60 Sec)	=	300°C

Test objective: Based on the technical features of the devices provided above the part maximum operating temperature is -40°C to 150°C. This part has been proposed to use in the actuator electronics that is to be used in a temperature range of –125°C to 90°C. Therefore, an assessment of the package is necessary prior to employ in such extreme low temperature environment.

Thermal Cycling Tests:

A thermal cycling chamber was used to assess the parts for their package robustness in a temperature range of –125°C to 90°C. This chamber has the capability to perform thermal cycling in a temperature range of –

196°C to 200°C. After optical inspection of the parts, which were loaded for thermal cycling. Figure 2 shows the optical photograph while loading the parts into the chamber. We have prevented the condensation by bringing the hardware to a warm temperature before opening the chamber. Dry nitrogen was continuously passed into the chamber to avoid condensation. Thermal cycling was performed using LabView in a remote mode. We have performed 10 thermal cycles from –125°C to 90°C as per the thermal profile (ramp rate of 7°C/min, dwell time ~12 minutes). Finally, the test was stopped at ~ 45°C. Optical inspection was performed after thermal cycling and unloading the parts. Figure 3 and 4 show the optical photographs of the parts (top side and bottom side) taken after thermal cycling in the inspection laboratory using optical and digital camera. The packages were intact (#621, 622, and 623) that are inspected. No cracking was observed even after 10 thermal cycles from –125°C to 90°C. This is based on external inspection of the packages only. Electrical and Non-destructive Analysis (NDE) analysis will provide substantial input on the characteristics of the parts. Figure 5 shows the close-up of the copper exposed area around the lead on one of the packages. The surface seems tarnished/black after thermal cycling test. This study requires an analysis of the copper surface by using Auger/XPS before and after thermal cycling. If there is any oxidation the signal corresponding to oxygen should increase. It may be worthwhile to implement the analysis of the exposed areas of the leads before and after thermal cycling in the future test runs on any packages.

In Summary – Analog Devices operational amplifiers were subjected to ten thermal cycles in the range of –125°C to 90°C. This temperature range is appropriate for a package where no thermal control was provided in a subsystem of the project. No cracks or damage was observed in the packages (number of packages/parts inspected: 3) after ten thermal cycles in an extreme low temperature range. Surface analytical techniques may be used in the future to characterize the surface of the leads before and after thermal cycling to learn more about the surface characteristics. X-ray and C-SAM may be used before and after thermal cycling in such extreme temperature range to learn more on the inside of packages that are being inspected using optical microscopy which is good only for external features.

Acknowledgements: Thanks are due to Shri Agarval, Mike Sander, Kevin Robinson, and Larry Elias for their help prior, during, and after thermal cycling test. Thanks are due to MER project and NEPP project support to assess the reliability of robustness of the package.

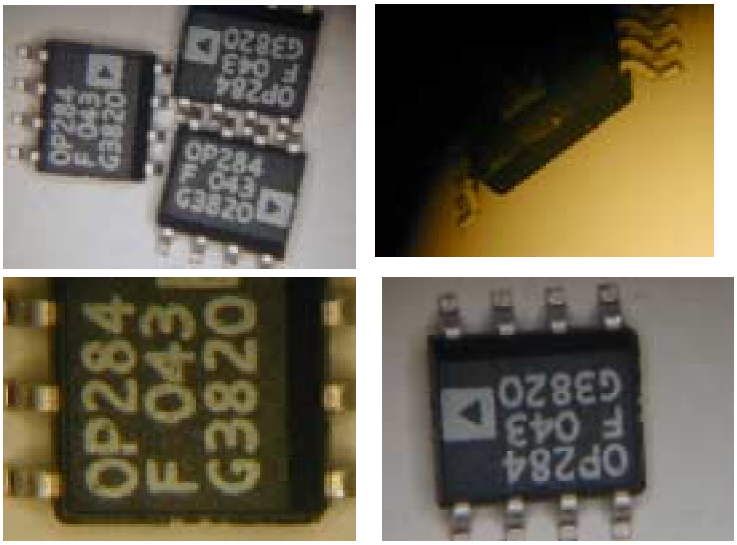
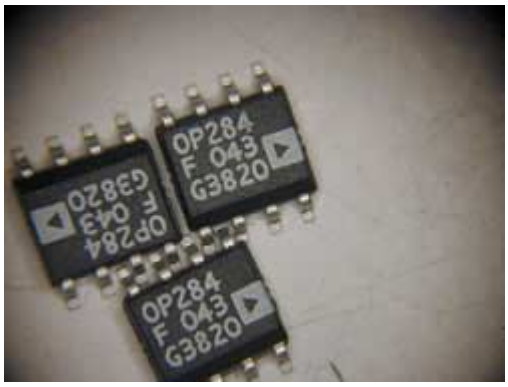
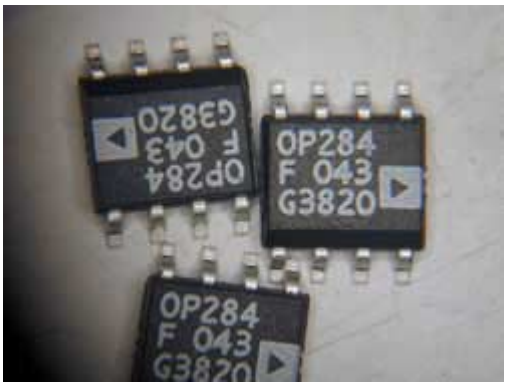


Figure 1: Optical photographs of the devices before thermal cycling

Figure 2: Loading of parts in the thermal chamber





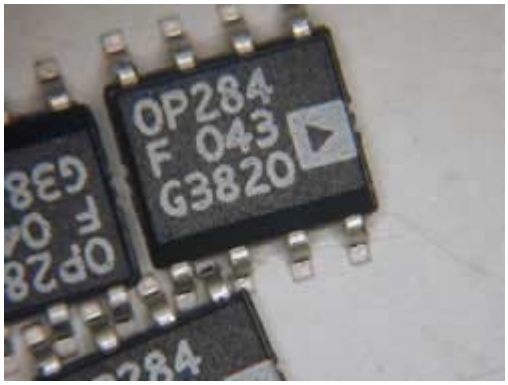


Figure 3: Optical photographs of parts after thermal cycling (top side)

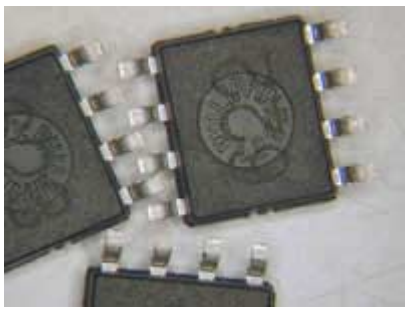


Figure 4: Optical photographs of parts after thermal cycling (bottom side)

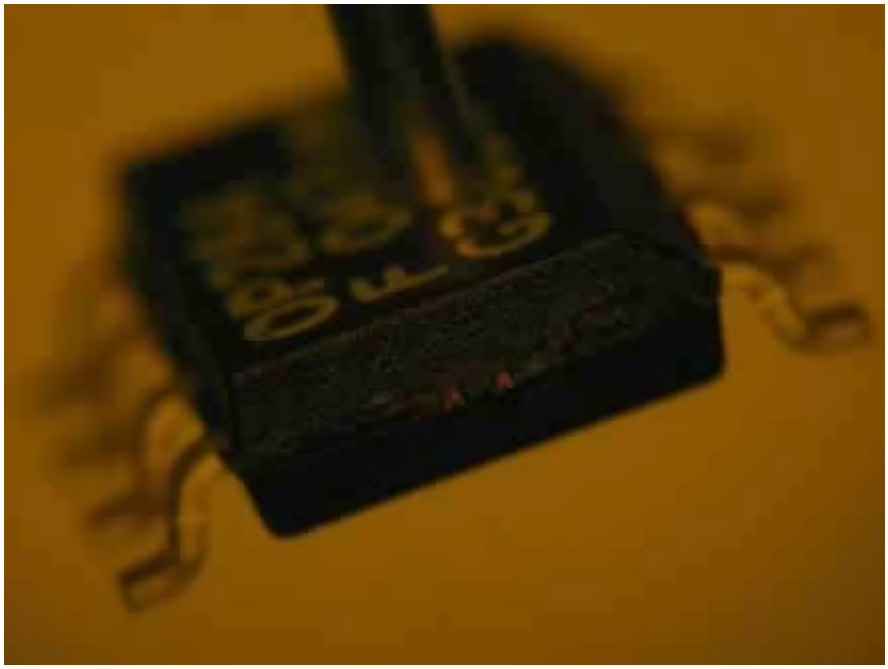


Figure 5: Optical photograph of exposure of copper

New EPIMS Tool to be Released Soon

Steve Waterbury
GSFC/NASA

Developers of NASA's EPIMS (Electrical, Electronic, and Electromechanical [EEE] Parts Information Management System) will soon release a desktop tool that will make using the system more convenient. The tool will enable users to import parts lists' into the system from spreadsheets and databases. Some of the other features that the new tool will provide are:

* importing parts list data directly from an Excel spreadsheet
  (without having to save the data to a tab-delimited file first)

* creating an "indentured" assembly structure of items
  (spacecraft, instruments, boxes, boards, etc.), and
  enabling parts lists to be attached to specified items in the
  assembly

The desktop tool will be made available initially to a small group of "beta" users. If you are interested in being one of the beta users, contact Steve Waterbury as soon as possible at (steve.waterbury@gsfc.nasa.gov).

Material System for Packaging 500°C SiC Microsystems

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Abstract

In order to establish a material system for packaging 500°C SiC microsystems, aluminum nitride (AlN) and aluminum oxide (Al_2O_3) were selected as packaging substrates, and gold (Au) thick-film materials were selected as substrate metallization material for electrical interconnection system (thick-film printed wires and thick-film metallization based wire-bond) and conductive die-attach interlayer. During a 1500-hour test in atmospheric oxygen with and without electrical bias, the electrical resistance of Au thick-film based interconnection system demonstrated low and stable electrical resistance at 500°C. The electrical interconnection system was also tested in extreme dynamic thermal environment. A silicon carbide (SiC) Schottky diode was attached to ceramic substrate using Au thick-film material as the conductive bonding layer and was successfully tested at 500°C in air for more than 1000 hours. In addition to the electrical test of die-attach in static thermal environments, nonlinear finite element analysis (FEA) was used for thermal mechanical evaluation and optimization of the die-attach in a wide temperature range.

1. Introduction

NASA is interested in using high temperature operable microsystems, including micro-electro-mechanical-systems (MEMS) and on-chip electronics, to characterize *in-situ* combustion environments of aerospace engines and the atmosphere of inner solar planets such as Venus. As an example, high temperature pressure sensor is one of NASA and aerospace industry's 'most wanted' high temperature sensors for application in development of new generation of aerospace engines. The sensor and on-chip electronics must operate at temperatures up to 500°C, and the devices are always directly exposed to combustion species including oxygen in air, hydrocarbon/hydrogen in fuel, and catalytically poisoning species such as NO_x and SO_x in combustion exhaust. The temperature in the atmospheric environment of Venus is also as high as 500°C, and its gas ambience is corrosive. These operation environments can be summarized as high temperature, high dynamic pressure, and chemically corrosive. Various SiC semiconductor devices have been demonstrated to be operable at temperatures as high as 600°C [1,2], but only in a probe-station test environment partially because chip level packaging technology for high temperature (500°C and beyond) devices is still being developed. Core technologies needed for successful high temperature device packaging include high temperature operable electrical interconnection system and a conductive die-attach scheme.

MEMS devices, as they are identified, are both electrical and mechanical devices. Through micro-level mechanical operation, MEMS devices, as sensors, may transform mechanical, chemical, optical, magnetic, and other non-electrical parameters to electrical/electronic signals. As actuators, MEMS devices transform electrical/electronic signal into non-electrical/electronic operation. Therefore, compared to conventional integrated circuit (IC) packaging, the most distinct issue of high temperature MEMS packaging is to meet the thermal mechanical requirements imposed by the mechanical operability and reliability of MEMS devices in a wide temperature range. High temperature SiC piezoresistive pressure sensors is a good example to illustrate the thermal mechanical requirements for packaging high temperature MEMS: the sensing mechanism of this

device depends on the mechanical deformation of the semiconductor resistors residing on a diaphragm fabricated by micro-machining. Therefore, this device is very sensitive to the thermal mechanical stress from the die-attach due to mismatches of coefficients of thermal expansion (CTEs) in the die material (such as SiC), the substrate material, and in the die-attaching material.

Since MEMS devices have very specific structure requirements with respect to their immediate packaging environment [3], it is expected that the design of MEMS packaging will be very device dependent. This is in contradiction to the conventional IC packaging practice in which a universal package design can accommodate many different ICs. In order to address the common needs of high temperature microsystem packaging, we first discuss the basic requirements for packaging materials. Based on the discussions on the material requirements, a gold thick-film metallization based 500^{o}C operable electrical interconnection system and a thick-film material based conductive die-attach scheme are introduced. Following that the thermal mechanical evaluation and optimization of the die-attach are addressed by nonlinear finite element analysis (FEA).

2. Material Requirements

A summary of basic requirements of the major materials needed for packaging high temperature microsystems may help to establish guidelines for material selections:

Substrates: Ceramics meet the basic requirements for substrate material to be operable at high temperatures since ceramic materials have excellent and stable chemical and electrical properties at high temperatures, especially, in corrosive gas ambience. After a substrate material is selected, a high temperature operable metallization scheme (both materials and processing) matching the substrate material must be identified or developed to provide electrical interconnection. In order to reduce the thermal mechanical stress of the die-attach structure, the CTE of substrate material must match that of the device material (such as SiC). The properties of substrate surface and the interfaces formed at high temperature with other packaging materials, such as the die-attach material, also become very important. At high temperatures, the surfaces of some ceramics gradually react with gas ambience, such as oxygen and water vapor, therefore, would exhibit changes in properties such as surface resistivity and surface adhesiveness to other materials.

Al_2O_3 has excellent electrical properties and chemical/electrical stability at high temperatures so it is a candidate substrate material for high temperature operation. In comparison with Al_2O_3, AlN has a higher thermal conductivity and a lower CTE which is close to that of SiC, so it is a good substrate material for packaging SiC high temperature and high power devices. The CTEs of α and β polycrystalline SiC are very close to that of single crystal SiC, so thermal-mechanically they are ideal substrates for packaging large SiC die for operating in a wide temperature range. However, both the dielectric constants and the dissipation factors of these materials are relatively high [4]. In order to be used as a packaging substrate, the surface properties of polycrystalline SiC must be modified. After appropriate surface modification these materials might still be suitable only for low frequency application because of their high dissipation factors. Based on these discussions, AlN and 96% Al_2O_3 were selected as high temperature substrate materials.

Metallization/Electrical Interconnection System: Most metals and alloys oxidize at temperatures near 500^{o}C in air. So the metals and alloys commonly used in conventional IC packaging such as copper, aluminum, and gold/nickel coated Kovar are excluded from packaging applications at temperatures of 500^{o}C and above unless a perfectly hermetically sealed inert/vacuum environment is available. At temperatures above 200^{o}C, intermetallic phases form at the interface of metals, such as Al and Cu. An intermetallic phase very often reduces the mechanical strength of the interconnection system. Thus, achieving material consistency in an interconnection system becomes extremely important in order to avoid thermal mechanical failure at high temperatures.

Precious metals are naturally considered for substrate metallization and electrical interconnection materials because of their chemical stability and good electrical conductivity. But some precious metals, such as platinum (Pt) and palladium (Pd) react with atomic hydrogen (H) to form H rich alloy at elevated temperatures. Though this is desirable for gas sensing devices [5], it is not so for electrical interconnection applications, because the phase transition may cause significant changes in the physical and electrical properties of these metals. Gold (Au) is extensively used for both substrate metallization and thin wire-bond in packaging and hybridizing conventional ICs. Besides the high conductivities and superior chemical stability at high temperatures, Au also has a low Young's modulus and a narrow elastic region. As it will be discussed in the Conductive Die-attach section, these features of Au are helpful to reduce thermal stress generated at the Au/die and the Au/substrate interfaces due to CTE mismatches if Au thick-film material is used as die-attaching interlayer. These features of Au are especially important to packaging high temperature MEMS because a wide range of operation temperature is of concern and the thermal mechanical stress is critical to the reliability of the packaged device. It has been reported that Au thin film/wire with small grain size suffered from electro-migration of Au atoms at grain

boundaries at high temperature under extreme current density (~10^6 A/cm^2) operation [6]. Surface modification and coating were suggested for Au conductor in order to be able to operate at high temperature and high current density [6].

Conductive Die-attach: Generally, die-attach materials are expected to be electrically and thermally conductive and physically/chemically stable at high temperatures, and to permit a die attaching process at a temperature within the temperature range of device operation. For applications in high temperature MEMS packaging, the thermal mechanical properties of die-attach material such as CTE, Young's modulus, fatigue/creep properties, and their temperature dependencies are very much of concern since the die attaching material is in intimate contact, both electrically and mechanically, with the die and the substrate. The die attaching material is, therefore, also expected to thermo-mechanically compensate for any possible CTE mismatch between the die and the substrate materials. Another major concern of die-attaching materials for high temperature application is long-term chemical and mechanical stabilities of its interfaces formed with the die and substrate materials at high temperatures. If the die-attach is expected to be electrically conductive, the electronic properties of its interface with the die would also become critically important. Combining all these mechanical, chemical, and electrical requirements, it is apparent that a material system for die-attach with a suitable attaching process is critical to the success in packaging high temperature MEMS device.

The thermal mechanical stress of the die-attach due to the mismatches of CTEs of the die, the attaching material, and the substrate may cause degradation and failure of packaged devices. The extreme case of die-attach failure caused by thermal mechanical stress is cracking of the die or the attaching material. For high temperature MEMS devices, besides the failure due to fatigue and creep in the die and attaching materials, thermal stress can also cause undesired device thermal response, irreproducibility of device operation, and output signal drift. Therefore, the thermal mechanical failures of the die-attach due to material CTE mismatches are expected to be common and important thermal mechanical issues which need to be addressed in packaging MEMS devices, especially high temperature MEMS devices.

3. High Temperature Electrical Interconnection System

As discussed in the last section, 96% Al_2O_3 and AlN are selected for substrate materials because of their high temperature chemical and electrical stabilities. Au thick-films provide basic chemical and electrical stabilities at high temperatures [7,8], therefore are selected for metallization and wirebond. In this section we discuss an Au thick-film based 500^{o}C operable electrical interconnection system for packaging low power high temperature microsystems.

Au thick-film was screen-printed on a ceramic substrate (AlN or 96% Al_2O_3) and cured at 850^{o}C in air using the recommended curing process [9], to form printed wire and metallization pads for wire-bond. In order to examine the high temperature stability of the printed thick-film circuit, the test circuit was electrically tested at 500^{o}C in air for a total of ~1500 hours using four probe resistance measurement. The electrical resistance of the thick-film wire/circuit was first measured at room temperature, then the temperature was ramped up to 500^{o}C for ~1000 hours without electrical current flow and the resistance of the wire was measured periodically. The resistance fluctuated slightly within 0.1% during the first 1000 hours test, as shown in Figure 1. After testing for 1000 hours without electrical bias, the circuit was biased with 50 mA DC current and the resistance was continuously monitored. The resistance fluctuated slightly within 0.1% for 500 hours with electrical bias. This very small change in resistance is acceptable for almost all envisioned high temperature device packaging applications.

Figure 1: Normalized resistance of thick-film wire at various temperatures with and without DC

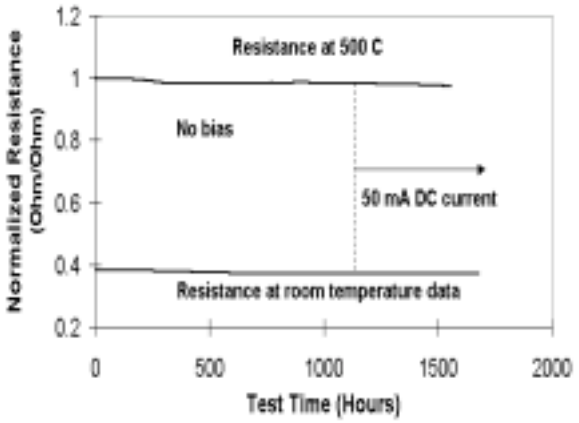
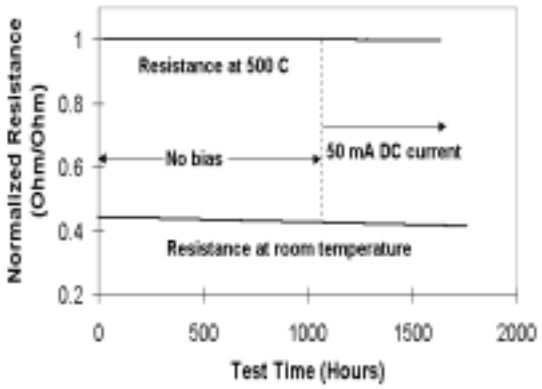
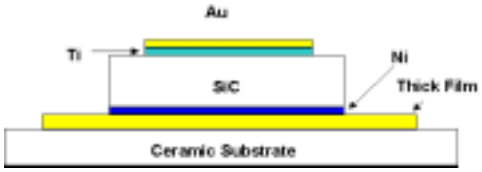


Figure 2: Normalized resistances of wire-bond test circuit measured at room temperature and 500°C vs. test time at 500 °C with and without DC bias.



In addition to the high temperature electrical validation discussed above, the Au thick-film metallization system needs to be mechanically evaluated at high temperatures in order to be reliably applicable at elevated temperatures. The tensile strength of Au thick-film metallization on 96% Al_2O_3 substrate has been tested at room temperature after extended storage at 500°C [7,10]. In order to examine the mechanical strength and the thermal dynamic stability of the binding system of Au thick-films at high temperature, the shear strength of Au thick-film metallization on 96% Al_2O_3 substrate was tested at temperatures up to 500°C. The shear strength (breaking point) at 500°C reduced by a factor of ~ 0.80 with respect to that at 350°C while the shear strength (breaking point) at 350°C was close to that at room temperature. The shear strength of Au thick-film designed for AlN were not as high as those for Al_2O_3, but it was sufficient for application in microsystem packaging operable at 500°C.

Figure 3: Schematic diagram of as - fabricated SiC device and die-attach structure.



After the electrical and mechanical qualifications of Au thick-film metallization on Al_2O_3 and AlN substrates, the electrical stability of thick-film metallization based wire-bond test circuit [9] including thick-film conductive wire/pads, bonded thin Au wires, and the interfaces between them were extensively tested at high temperature with and without electrical bias in oxidizing air. The test sample is composed of 22 units of 1 mil Au wire-bond (44 bonds) in series. The resistance of the wire-bond sample was measured at room temperature and 500°C at various testing times at 500°C. The resistance was first measured at room temperature, followed by ramping the temperature up to 500°C and the resistance was monitored in air without electrical bias for 670 hours. As shown in Figure 2, the temperature was then lowered back to room temperature and the resistance was recorded again. After this thermal cycle, the circuit resistance was continuously monitored for a total of 1200 hours at 500°C in air without electrical bias (current flow), followed by another 500 hours at 500°C with 50 mA (DC) current. The resistances under all these conditions were desirably low (less than 0.5 Ω per unit) and decreased slowly and slightly at an average rate of 2.7% over the 1500 hour testing period. The rate of resistance decrease under the DC bias is close to that without electrical bias.

An identical wire-bond circuit of that tested in static thermal environments was electrically tested in dynamic thermal environment. The wire-bond circuit was tested under thermal cycles between room temperature and 500°C with an initial temperature rate of 32°C/min for 123 cycles first, then at the temperature rate of

53°C/min (higher than thermal shock rate) for additional 100 cycles with 50 mA electrical bias. The maximum change in electrical resistance during the thermal cycles is 1.5% at room temperature, and 2.6% at 500°C [11].

4. Conductive Die-attach

An Au/Ti/SiC Schottky diode with a Ni ohmic contact on the backside was used as a device to test the die-attach scheme developed for high temperature operation [12]. After dicing, the 1 mm x 1 mm SiC diode chip was attached to a ceramic substrate (either AlN or 96% Al_2O_3) using Au thick-film material as shown in Figure 3. This Au thick-film die-attaching scheme resulted in a low resistance die-attach which is necessary for packaging many devices with vertical topologies.

The optimum process for attaching SiC dies (with Ni contact) to the ceramic substrate was investigated. The thick-film uniformity issue needs to be addressed first. As discussed elsewhere [12], the organic vehicle of "raw" thick-film materials evaporates during the initial drying process. Since the thick-film material is sandwiched by the ceramic substrate and the SiC die, the escaping organic vehicle molecules have a relatively long way to migrate to escape from
the sides. During rapid drying this may distort somewhat the thick-film distribution, therefore, cause non-uniform thick-film distribution between the die and the substrate. A slower drying

process (120°C – 150°C) was critical to keep the thick-film bonding layer uniform and the die parallel to the substrate after the curing process. It was also necessary to consider reducing the amount of organic vehicle evaporated during die-attach processing. A two-step die-attach process was used. A thick-film layer was first screen-printed on the substrate and cured at 850°C, the SiC die was then attached to the cured thick-film pattern with minimal amount of subsequent thick-film.

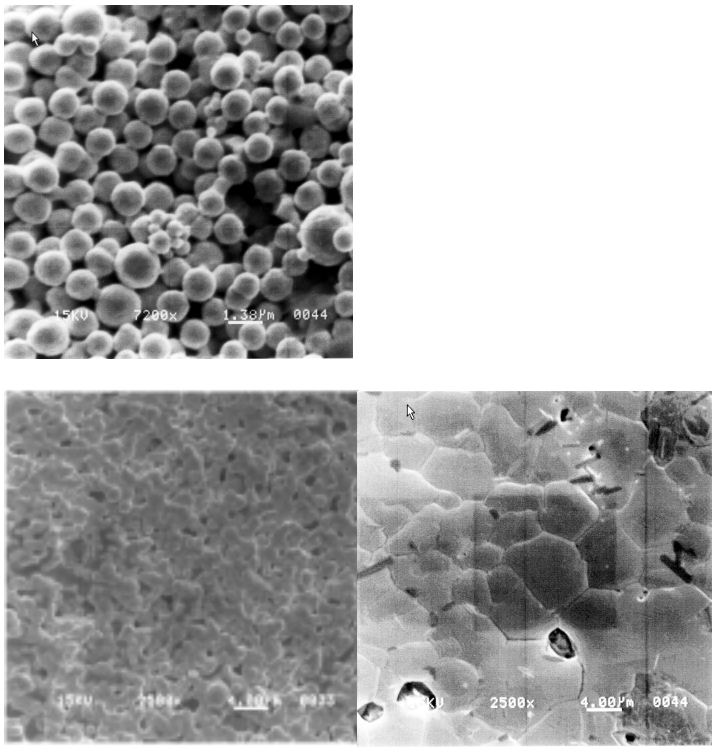


Figure 4, Scanning Electron Microscope (SEM) micrograph of thick film surfaces cured at (a) 500°C for 25 min, (b) 600°C for 20 min, and (c) 850°C for 15 min. (a) Micro powder structure indicating insufficient boundary diffusion. (b) Chain structure replaces powder structure indicating a critical curing condition. (c) A large and smooth grain structure indicating solid film formation.

The second processing parameter to be optimized is the final curing temperature. A lower final curing temperature (with respect to standard curing temperature of 850°C) was desired in order to minimize the curing

effects on the interfacial properties of Au/Ti/SiC device. To determine an optimized final curing temperature for the die-attach process, micro-structures and surface compositions of the thick-film cured at various temperatures were investigated. As shown in Figure 4a, the surface of thick-film cured at 500^{o}C showed very sharp Au micro powder structures indicating that there was insufficient diffusion to form a solid film at this temperature. The thick-film surface cured at 850^{o}C (Figure 4c) showed large grain sizes and a relatively smooth surface indicating thick-film formation. The thick-film surface cured at 600^{o}C (Figure 4b) showed that micro powder structure has been replaced by net and chain structures indicating a critical curing condition necessary for formation of a coherent thick-film. Based on this result, 600^{o}C was selected as the preferred final die-attach processing temperature. Auger Electron Spectroscopy was used to characterize the surface compositions of the thick-film surfaces cured at 500, 600, and 850^{o}C. In addition to expected normal levels of carbon and oxygen surface contaminations, copper and lead (oxides as binders) were found on the surfaces of all three samples. Compared to the sample surfaces cured at 500 and 600^{o}C, binder concentrations on the sample surface cured at 850^{o}C were relatively lower indicating high curing temperature is preferred for binder molecules migration to the interface with ceramic substrate. So the first layer of thick-film screen-printed on the substrate was cured at 850^{o}C for best adhesion. Since the thick-film material used as die-attach binding materials 'sees' metals on both sides (Au thick-film on the substrate and the Ni thin film on the backside of the SiC die), it seems less likely that the binders should significantly segregate to the interfaces. A 0.001'' diameter Au wire was bonded on the top Au thin-film metallization pad with a thick-film overlayer by thermal-compression bonding technique. Thick-film material was also used to reinforce the top Au thin film for better wire bonding. The Au thin-film metallization area was coated with thick-film on the top then dried at 150^{o}C for 10 minutes. The thick-film on the device top was cured during the final die-attach process (at 600^{o}C).

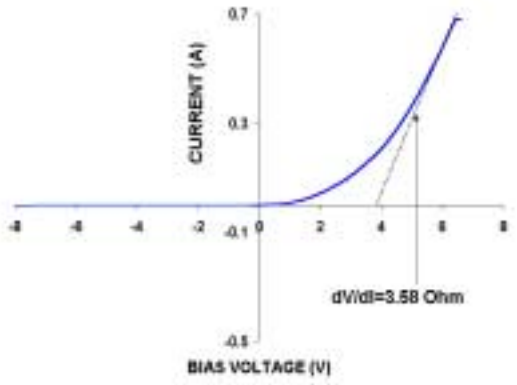


Figure 5: I-V curve of attached SiC test-diode characterized at 500 ^{o}C after being tested for 1000 hours at 500 ^{o}C oxidizing air.

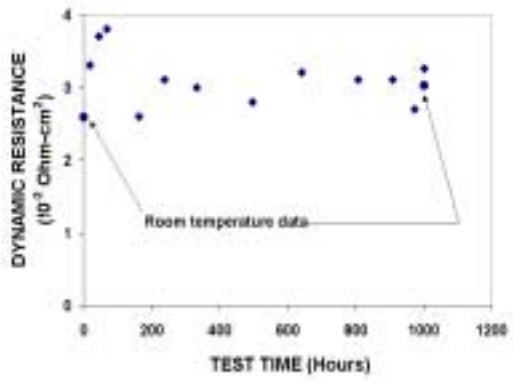


Figure 6: Minimum specific dynamic resistance (normalized to device area) calculated from I-V data vs. heating time at 500 ^{o}C. This resistance includes resistances contributed from the Au(Ti)/ SiC rectifying interface, SiC

wafer, the die-attach materials/ interfaces. Resistances of the bonded wire and the test leads have been subtracted.

The attached SiC test diode (Figure 3) was characterized by current - voltage (I-V) measurements at both room temperature and 500°C for various heating times. A minimum dynamic resistance (dV/dI) in a high current (forward biased) region of the I-V curve was used to estimate both the stability and the upper limit of resistance of the die-attach structure (both interfaces and materials), as shown in Figure 5. This dynamic resistance includes forward dynamic resistance of Au/Ti/SiC interface, SiC wafer bulk resistance, the die-attach materials/ interfaces resistance, bonded wire resistance, and the test leads resistance in series. The resistance contributed from test leads and bonded wire were measured independently and subtracted. The attached device was first characterized by I-V measurements at room temperature. The device exhibited rectifying behavior and the minimum dynamic resistance after subtracting test-leads/bond-wire resistance (applies to all the following discussion) measured under forward bias was ~ 2.6 Ω, as shown in Figure 7. The temperature was then ramped up to 500°C (in air) and the diode was *in situ* characterized periodically by I-V measurement for ~1000 hours. During the first 70 hours at 500°C the (lowest) dynamic resistance under forward bias increased slightly from 3.3 Ω to 3.8 Ω. After that the dynamic resistance decreased slightly and remained at an average of 3.1 Ω. The diode was then cooled down to room temperature and characterized again. The minimum forward dynamic resistance measured at room temperature was 3.3 Ω. It is worth noting that the device's I-V curve changed somewhat with time during heat treatment at 500°C. However, the dynamic resistance of attached diode remained comparatively low over the entire duration of the test and temperature range, indicating a low and relatively stable die-attach resistance.

AlN material properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	3.14	50.00	0.25
20	3.90	50.00	0.25
105	5.36	50.00	0.25
205	6.51	50.00	0.25
305	7.25	50.00	0.25
405	7.76	50.00	0.25
505	8.25	50.00	0.25
605	8.72	50.00	0.25
705	9.09	50.00	0.25

96% Alumina properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	5.34	44.00	0.21
20	6.20	44.00	0.21
105	7.83	43.58	0.21
205	8.48	43.06	0.21
305	8.89	42.51	0.21
405	9.28	41.93	0.21
505	9.65	41.34	0.21
605	10.00	40.74	0.21
705	10.33	40.13	0.21

SiC material properties			
Temp (deg C)	CTE (xE-6/°C)	E (xE6 psi)	ν
-15	2.93	66.72	0.3
20	3.35	66.72	0.3
105	3.97	66.42	0.3
205	4.23	66.08	0.3
305	4.46	65.74	0.3
405	4.68	65.39	0.3
505	4.89	65.05	0.3
605	5.10	64.71	0.3
705	5.29	64.36	0.3

Au material properties			
Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	ν
-15	14.04	11.09	0.44
20	14.24	10.99	0.44
105	14.71	10.83	0.44
205	15.23	10.59	0.44
305	15.75	10.28	0.44
405	16.29	9.92	0.44
505	16.89	9.51	0.44
605	17.58	9.03	0.44
705	18.38	8.50	0.44

Table 1: Basic material properties of SiC, Au, 96% alumina, and AlN used for FEA simulation for die-attach structure.

5. Thermal Mechanical Properties of Die-attach

As it was discussed in Material Requirements section, the mechanical issues of most concern for high temperature MEMS packaging are the die-attach thermal stress problem and the general guidelines for material selection, structure design, and optimization of attaching process to minimize overall thermal stress of the die-attach structure. Assuming that a conventional die-attach structure, in which the die-backside is attached to a substrate using an attaching material layer, is adopted, the typical die-attach structure is illustrated in Figure 3. The die-attach using Au thick-film material discussed in last section is a typical example of this structure.

For high temperature microsystem packaging, thermal mechanical properties of the die-attach structure need to be addressed at two levels: 1) Mechanical damage of the die-attach structure resulting from thermal mechanical stress. 2) Thermal stress/strain effects on the mechanical operation of devices. The failures at both levels are rooted in thermal mechanical stress of the die-attach. The thermal mechanical governing equations [13] of the die-attach are complicated, but analytically solvable in some cases [14,15]. References 14-15 have investigated the design of the die attach assembly using closed analytical solution assuming linear elastic material properties. Nonlinear effects were also considered in a simplified model in reference 15. Considering the wide temperature range and low yield strength of gold thick-film, a non-linear elastic-plastic finite element analysis (FEA) was used to simulate Au thick-film based SiC die-attach as an example of die-attach optimization for packaging high temperature MEMS.

The basic mechanical properties of SiC, Au, AlN, and 96% Al_2O_3 and their temperature dependence used for FEA simulation are listed in Table 1 [11]. The temperature dependence of Young's modulus of AlN in a wide temperature range has not been reported, so it was extrapolated as a constant from the data at room temperature. Poisson's ratios of both single crystal 4H-SiC and AlN are not published, so they were estimated according to those of other carbides and nitrides. The thermal and mechanical properties of 4H SiC were assumed isotropic. Since the yield strength of Au thick-film material has not been published, the simulation was conducted in a range of yield strength from 650 to 3000 psi. The numerical calculation using the yield strength at the low end diverged.

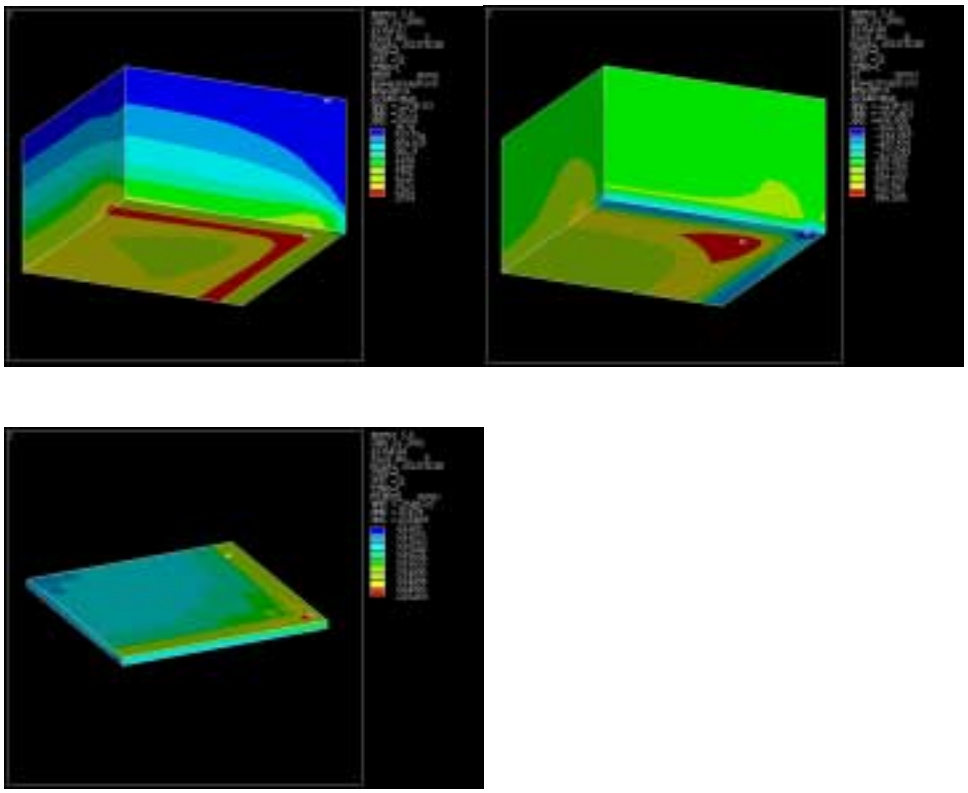


Figure 7: Thermal stress and strain distribution in SiC die and Au thick-film layer at room temperature, the relaxing temperature is 600^{o}C. (a) Von-Mises stress distribution in SiC die. (b) Maximum Principal Stress distribution in SiC die. (c) Equivalent Plastic Strain in Au thick-film layer.

Figure 7(a) and (b) show Von-Mises stress and Maximum Principal Stress contours of a quarter of SiC/Au/AlN die-attach structure at room temperature with relaxing temperature of 600^{o}C. Horizontally, at the interface with a Au thick-film layer, the stress in the die basically increases with the distance from the center of the die attach interface, the stress reaches a maximum at the area close to the die edges, especially, at the corner. This is understandable. The source of thermal stress of the die-attach structure is CTE mismatch at bonding interfaces. At the area far from the neutral point (larger distance from neutral point, DNP) the trends of relative displacement with respect to Au thick-film, driven by the CTE mismatch, would be larger. From this it can be predicted that the maximum thermal stress would increase tremendously with increase of the die-size, or attaching area. Vertically, the stress attenuates rapidly with the distance from the interface. At the die center region the stress near die surface attenuates by a factor of 1/80 with respect to the stress at the interface. With this picture of thermal stress distribution one can conclude that flip-chip bonding would not be recommended for high temperature MEMS devices if the CTE mismatch is not well controlled, and a thicker die (or a stress buffer layer of the same material) can significantly reduce the thermal stress at die surface region.

Figure 7(c) shows Equivalent Plastic Strain (EPS) in the Au thick-film layer. Because of the same physical mechanism as that for SiC die, the highest EPS in Au layer are located at the area close to the corner, where the DNP is larger. This indicates that smaller die-size/attaching-area may provide relatively better thermal mechanical reliability with respect to larger dies.

In comparison with AlN substrate, 96% Al_2O_3 substrates have relatively higher CTEs (~6.2×10^{-6} / ^{o}C compare with ~3.9×10^{-6} / ^{o}C of AlN). The FEA results indicate that using AlN substrate would result in an improvement of maximum Von-Mises stress in SiC die by a factor of 0.29, an improvement of Von-Mises stress in the substrate by a factor of 0.33, and an improvement of MPS in Au thick-film layer by a factor of 0.42. This improvement of thermal stress/strain corresponds to an improvement of fatigue lifetime of Au thick-film layer by a factor of 4.3 – 9.0 (assuming the power law exponent in Coffin-Mason model, C, is -0.4 and -0.6, respectively). So in terms of thermal mechanical reliability of die-attach, AlN is suggested for packaging SiC high temperature MEMS devices compared to 96% Al_2O_3 owing to the fact that the CTE of AlN is close to that of SiC.

Figure 8 shows maximum Von-Mises Stress in substrate and SiC and the EPS of the thick-film layer vs. the thickness of Au attach layer. The maximum stress in the SiC die decreases by a factor of 0.75 with respect to the thickness change from 20 μm to 50 μm, for AlN substrate, while the maximum stress in the SiC die decreases by a factor of 0.5 with respect to the thickness change from 20 μm to 50 μm, for 96% Al_2O_3 substrate. The increase of Au layer thickness also significantly improves the stress in AlN substrate, as shown in Figure 8(b). Figure 8(c) shows the maximum EPS in Au layer vs. thickness of Au attaching layer. The increase of the thickness from 20 μm to 50 μm significantly reduces the EPS in the Au thick-film layer in both AlN and Al_2O_3 cases.

Besides the dependence of thermal mechanical configuration of the die-attach on material properties of the die, the attaching layer, and the substrate, the thermal mechanical stress in a die-attach structure also depends on the temperature deviation from the relaxing temperature, T_R, at which the structure is thermal-mechanically relaxed [13,16]. In order to assess the relaxing temperature effects on the thermal stress of the die-attach structure, the stress distribution of the die-attach at room temperature is simulated by FEA assuming that the structure is relaxed at various temperatures (from 300 - 600^{o}C). Figure 9 shows the maximum Von-Mises stress in the die and EPS in Au thick-film layer vs. the relaxing temperature. If the relaxing temperature could be lowered from 600^{o}C to 300^{o}C, the maximum Von-Mises Stress in the die can be reduced by a factor of 0.8. And the maximum EPS in Au thick-film layer can be reduced by a factor of 0.5. The fatigue lifetime corresponding to the stress reduction is improved by a factor of 3 (assuming the exponent in Coffin-Mason model of fatigue, C, is -0.6). Ideally, the thermal mechanical property of the die-attach structure is optimized if the relaxing temperature could be set at the middle of the operation temperature range.

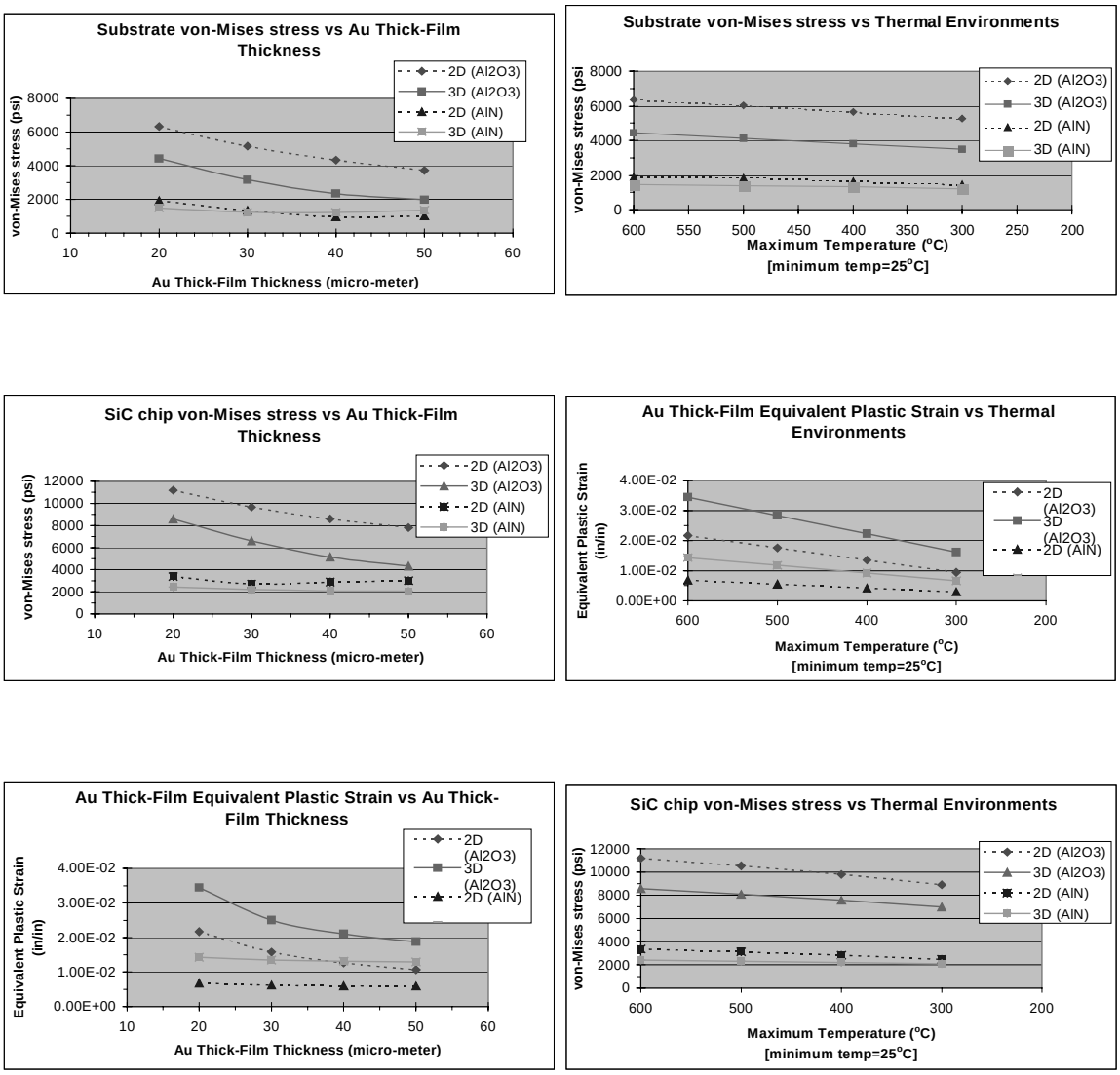


Figure 8**:** Maximum stress and strain of die-attach vs. the thickness of Au thick-film interlayer, at room temperature. (a) von-Mises stress in AlN substrate, (b) von-Mises stress in SiC die, and (c) EPS in Au thick-film

Figure 9: Relaxing temperature dependence of maximum stress and strain in SiC chip, substrate, and Au attaching layer.

6. Summary and Discussion

Ceramic substrates, Al_2O_3 and AlN, and Au thick-film metallization based material system were discussed for low power high temperature chip level packaging. The electrical interconnection system of this packaging system has been extensively tested in a temperature range from room temperature to 500°C with and without electrical bias in oxidizing environments. The mechanical strengths of Au thick-film metallization on both Al_2O_3 and AlN substrates have been preliminary tested at 500°C. Following electrical and mechanical tests in static thermal environments, the Au thick-film wire-bonds were evaluated in extremely dynamic thermal environments from room temperature to 500°C. The test sample including 44 Au wire-bonds, survived 120 thermal cycles at temperature rate of 32°C/min and 100 additional cycles at 53°C/min in oxidizing environment with 50 mA DC current which is sufficient for many low power devices. An attached SiC diode using this technology was successfully tested at 500°C in an oxidizing environment for more than 1000 hours setting lifetime records for high temperature electronic packaging.

In order to optimize the thermal mechanical properties of Au thick-film material based SiC die-attach, nonlinear FEA was used to simulate and compare the thermal mechanical stress/strain distributions against material,

structure, and processing parameters to establish basic guidelines of material selection, structure design, and processing parameters determination.

The combination of versatile functions of MEMS devices and survivability/operability at high temperature introduces a new generation of micro-devices, high temperature MEMS, with revolutionary capabilities for many aerospace applications. Packaging these revolutionary devices, however, presents new challenges and research in device packaging. In meeting these challenges, innovative packaging materials possessing superior physical/chemical properties suitable for high temperature operation, innovative structure/design meeting these specific device and operation requirements, and innovative packaging processes able to accommodate both the new materials and the new structures are expected.

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DEPARTMENTS

Up Close With David Beverly and Curt Tallman

David Beverly, NASA Johnson Space Flight Center International Space Station Team Lead for EEE Parts

Curt Tallman, Boeing EEE Parts Lead Engineer for the International Space Station

EEE Links – What are the new materials/technologies that are using Space Station as a test-bed?

Tallman – Space Station is not really a test bed for new technologies, instead we try to use mature and proven parts for our core systems. All the basic computing systems, communication systems, data systems are using proven technology and we're not out on the edge of technology trying to innovate too much. This is particularly important when you have a 15 year program and must guarantee reliable operation given an ionizing radiation environment. As the number of experiments increases on Station then I am sure we will be using new technologies to capitalize on their advantage of expanded function, less power and much smaller size. I would hope we could work with the other centers to fly experiments that are using leading edge parts in an effort to see how well they perform against the reliability models for radiation and performance.

Beverly – Typically, we are not pushing technology in our manned space programs. In a rare case there is a hardware requirement that won't fit into the standard **SSQ 30312** EEE parts requirement plan and we start pushing the envelope a little bit, but we really haven't done that much because we want proven technology. One area where JSC is experimenting a little is the government furnished equipment (GFE) side of Station where we are using some commercial parts and off-the-shelf (OTS) hardware for low criticality applications. The challenge is to be able to accept OTS or commercial grade parts and come up with a reliable way of proving the hardware will work in low earth orbit.

Tallman – And we're not as power or space constrained as some of the satellites…things of that nature.

Beverly – We have pushed technology in a few areas, a good example would be on the DC to DC converter unit (DDCU). The initial part that was chosen happened to be from a qualified military manufacturer, but it began having reliability issues during field testing. This device is handling a hundred amps and hundreds of volts. So given little time to fix the problem, the team went to an existing commercial part that was encapsulated in plastic. Boeing went to great lengths to insure the part would be reliable and thoroughly screened and qualified it for its

tough environment. They're flying up there right now and so far we have had no problems. This approach went against the traditional wisdom by using a commercial part in a critical application.

Tallman – The DDCU box was basically a class B+ or class S minus level box. We ended up with a 100 Amp diode in there that has a die that was manufactured in Oregon, but the part was assembled in a plastic encapsulated case in the Philippines. We were able to buy them almost by the carload. The manufacturer had plenty of them and they were, as parts go, very inexpensive. We took a bunch of them and went through a very intensive qualification program and they worked very, very well. They passed our qualification program and now they've been in use and we are flying them in orbit. We've had no problems with them either in the box level testing and qualification or in orbit. So it shows that you can, with proper care, take some off the shelf parts and apply them in a low earth orbit application and apparently have a reliable product.

Beverly – At the same time, we cannot turn a sow's ear into a silk purse. We have to have a well-designed high quality part to begin with. All of the screening that was done, which was considerable, couldn't change what it basically was to begin with. Given the Station's 15 year plus mission, a poor quality part or an incorrectly selected part, will be nothing but trouble down the road.

EEE Links – How do you envision the role of advanced parts and packaging technologies and usage in Space Station evolution, over the next decade?

Beverly – We're seeing an evolution now as was mentioned earlier. The selection of leading edge or even several year old technology parts are hard to find on the qualified products list (QPL). We're moving more to commercial parts. Military parts are going to be rare and we're going to find high reliability commercial devices that will take their place. Technology is evolving so fast that it is not cost effective for a manufacturer to develop and qualify military grade parts with such limited sales potential. Since our options are decreasing I see us moving more and more to industrial grade parts as we redesign Space Station systems over its life. So as we do that, we are going to have to create a new set of requirements and test methods to allow us to use commercial parts in an extreme environment. Not only will the EEE parts engineer for Space Station need to change, we're all going to have to evolve if we are to continue to be successful in the space business.

Tallman – One of the things that I think you should note, is that for those electronic items that are maintained inside the pressurized environment of the Station the environment is not all that extreme. The temperature, humidity and pressure are all as it is, basically, here on earth. We don't have convection cooling, so we have to be a little more conserative in our power dissipation specifications. We still have some radiation environment inside, even though there's quite a bit of shielding provided by the skin of the Station and also some of the internal systems have their own metal and outer shielding. The external hardware like the multiplexer/demultiplexers (MDMs) are actually mounted on the outside of the pressurized mating adapter, so they are subject to quite a bit of temperature fluctuation, as well as more of a hot belt radiation environment. In order to keep things from getting too cold, we do have heaters for external hardware. A lot of electronic parts will not operate correctly if we let them get much below minus 50 or 60 degrees centigrade. But, on the other hand, there seems to be a lot of parts available that can handle the environment out there. The big thing has been radiation, so we have to go to more radiation hardened and proven parts.

EEE Links – Which leads me to my next question. Has Space Station experienced any anomalies, failures, or memory/logic upset that can be attributed to Single Event Effects (SEE) in earth's radiation environment?

Beverly – If you look at the core hardware that we fly on Station, in the last year we have had some major solar flares that really might have shut down critical systems – but the primary Station functions performed flawlessly. I think that Boeing has done an excellent job in its design for radiation tolerance. Now if I look at some of the JSC provided and managed GFE we have had a few problems, but nothing that was not expected. We knew the risk for upset existed in some non-critical hardware and spares were flown to replace the hardware if problems did occur.

EEE Links - What role and impact do you think international participation will have in the development of Space Station activities in the future?

Beverly – I am concerned with the budget decreases that we are seeing. If the world could see how hard people are working here at JSC and around the program, hours and hours of uncompensated time. I think it becomes obvious that if we cut budgets anymore than they've already been cut, I don't know how we're going to get our job

done safely. So one of the alternatives is getting the world to buy into what we're doing. I think it builds their national pride and develops their space related engineering expertise, I am all for it.

EEE Links – How many people do you think are needed in order to do science?

Beverly – A minimum of six to seven people. I think that our partners have every right to have representatives on station and participate fully in as much science as can be achieved. The world needs to believe in the vision that Station brings. I think whoever got the international partners involved was visionary and I think it is the right thing to do. It also puts pressure back on the United States to keep funding Station because the rest of the world is depending on us to do our part. They're saying, "you better fund the CRV (Crew Rescue Vehicle) and a new Hab module". Without those additions, station is crew limited and our IPs will not be able to fully participate. We've been working with Government-Industry Data Exchange program (GIDEP) on the restrictions of passing information to our international partners driven by the International Traffic in Arms Requirements (ITAR) requirements. In the past we have restricted the information that passes on to them on parts that they buy from American manufacturers and I think this is very unfortunate. We recently were notified that GIDEP would allow us now to share an abbreviated copy of the ALERTS with our partners. In the future they can get a sense of what our problems are and prevent those same problems in their hardware. Sure they're going to get access to some "American" technology, but they are building hardware for Station and if they fail, Station fails. I think there's going to have to be an evolution in mindset to understand that everyone is up there to win together.

EEE Links – How can the NASA Electronic Parts and Packaging Program (NEPP) and NASA EEE Parts Assurance Group (NEPAG) support those activities?

Beverly – As we move more away from military parts and into commercial and leading edge technology packaging, as well as die, NEPP needs to do what it's doing right now and continue to do advanced packaging studies and qualifications. What's cost effective…what technologies are reliable…what technologies work in our extreme environments. I think that they can serve an important part in helping Station continue to evolve by understanding what technologies are in fact faster, better, and cheaper. So I think NEPP can play an important part. One of their weaknesses in the past has been sharing their information with those of us out in the trenches. JPL can have the smartest engineers in the world but if they don't share what they know with the folks building the hardware, it has little value. I see this as a real challenge to NEPP - how to disseminate the most important information in the least amount of required reading time. Providing a web-page address or presenting a paper at a symposium is not good enough.

NEPAG, provides an EEE parts issues forum. Of course, it's a lot more than just the weekly telecons we have. It provides a forum to discuss problems we are having and inquire if anyone else has seen that problem. We are sharing real-time problems so we all become aware of them and can, hopefully, work together on solving and preventing their impact on our hardware. NEPAG has several important goals/deliverables that will be good tools when they are complete. One that comes to mind is to develop a NASA commercial parts selection and qualifications guideline. In other words; how should Parts Engineers around NASA approach and approve the use of commercial parts and/or off the shelf hardware? That's one of the tasks that NEPAG has that's not going to be easy. We'll have to look carefully at existing documents and decide if it might be better to borrow someone else's guidelines. The EEE parts community does not have enough resources to duplicate efforts from other organizations.

DEPARTMENTS

Guidelines for EEE Links Article Submission

EEE Links is a quarterly publication. The next publication focus and date will be:

November 16th - System on Chip Technologies
Article submission deadline is October 9, 2001

Submitting articles for EEE Links is a great means by which information and knowledge can be transferred inside and outside of the NASA community.

EEE Links support the NASA Electronic Parts and Packaging Program (NEPP). The EEE Links Newsletter information will augment the electronic parts, packaging, and radiation technologies.

EEE Links publishes many types of articles that relate to Electronic Parts, Packaging, and Radiation. First consideration goes to articles that deal specifically with the NEPP program. We also consider articles outside of the NEPP program but related to electronic parts, packaging, or radiation.

The submitted articles can be on current efforts referencing status and completion date. Articles can be informal and be from one paragraph to three pages in length on the following subjects:

Current Events within the NEPP Program and Projects
Parts
Packaging
Radiation
Reliability Issues Concerning NEPP
New / Emerging Technology
Space Flight Hardware
Quality Assurance Issues

To submit an article, please send it in a text-only format, preferably Microsoft Word, to Nancy Ford at nford@qssmeds.com. Please provide a copy of the Article Submission Checklist, found on the NEPP website at http://nepp.nasa.gov/imd/eee_links/article_checklist.htm. Provide the following information with your article submission:

Abstract - This two to four sentence paragraph summarizes the key points to capture the readers attention.

Photo - EEE Links publishes photos of the authors. The image should be scannable or in .gif or .jpg format.

Biography - This should be between 50 and 75 words outlining the author's job, background, professional accomplishments, and other pertinent accolades or areas of interest.

Contact Information - The author must include his or her business address, phone, fax, and email address.

Notes and References - Most articles require some references, and some contain incidental information best treated as notes. Use brackets for references and superscripts for notes, then list the two groups separately at the end of the article. These should be numbered in the order they appear in the article, not alphabetically.

Additional Reading - Our readers appreciate pointers to relevant books and articles. List these at the end of the article in the same format as references.

Copyright - The author is responsible for obtaining any copyright releases or other releases necessary for their article. The releases should be forwarded to the EEE Links Editor.

Letters to the Editor

Limit letters to 250 words. Include your name, phone number, and e-mail address. Names are withheld from publication upon request. We reserve the right to edit for style, length, and content.

DEPARTMENTS

UPCOMING EVENTS

SPIE International Society for Optical Engineering Reliability, Testing, and Characterization of MEMS/MOEMS Conference

October 21-24, 2001, San Francisco, CA
For details, see web site: http;//www.spie.org/info/mf

2001 IEEE GaAs IC Symposium

October 21-24, 2001, Renaissance Harborplace Hotel, Baltimore, MD
For details, see web site: http://www.gaasic.org

10th NASA Symposium on VLSI Design

November 7-8, 2001, NASA Design Center, University of New Mexico
For details, see web site: http://www.mrc.unm.edu

Nonvolatile Memory Technology Symposium 2001

November 7-8, 2001, San Diego, CA
For details, see web site: http://nvm.jpl.nasa.gov

2001 Core Technologies for Space Systems Conference

November 28-30, 2001, Double Tree Hotel, Colorado Springs, CO
For details, see web site: http://www.spaceresearch.org